FIG. 1

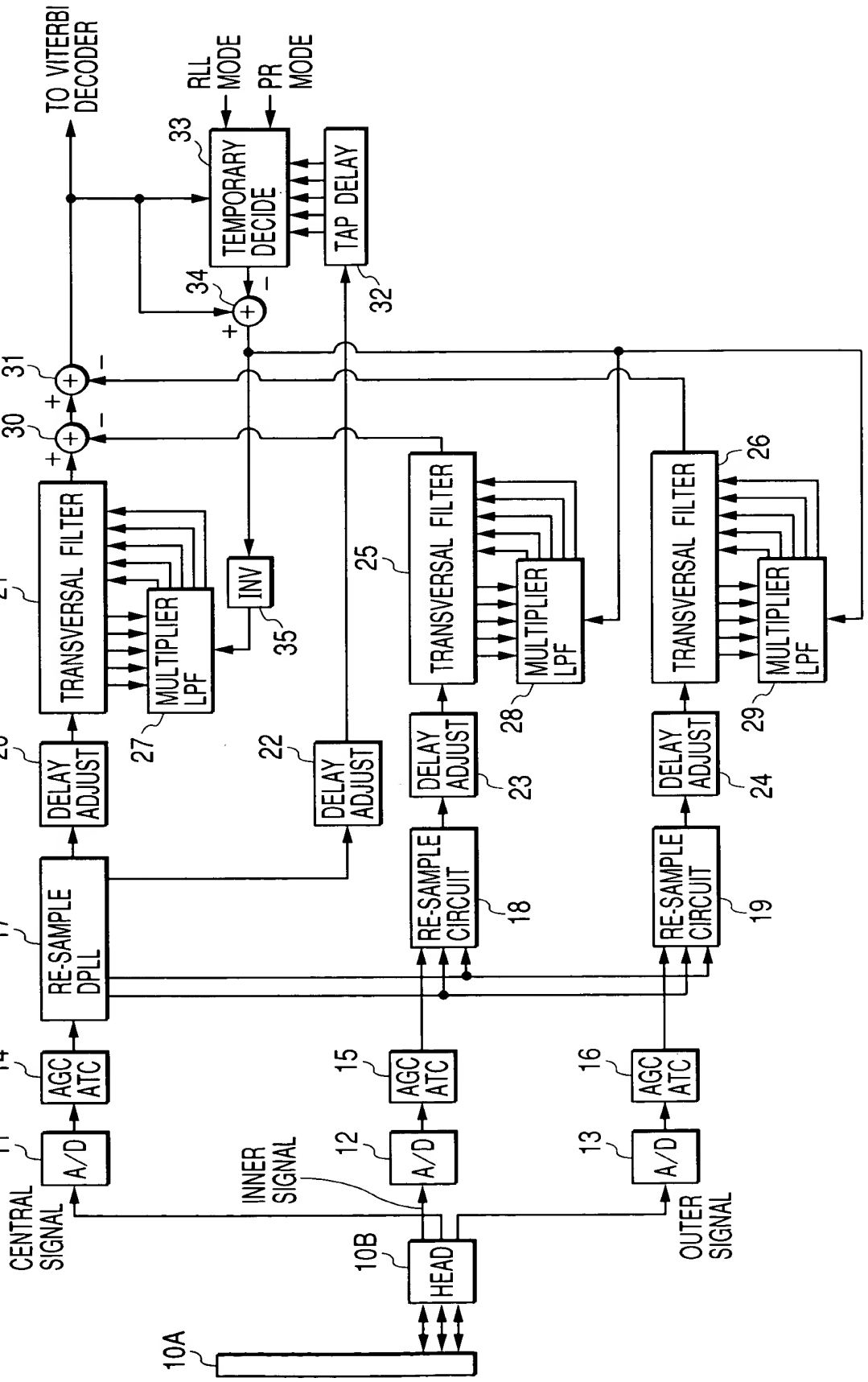

TO VITERBI DECODER
RLL MODE
PR MODE
33
TEMPORARY DECIDE
TAP DELAY
34
32
31
30
TRANSVERSAL FILTER
MULTIPLIER LPF
INV
35
21
27
20
DELAY ADJUST
22
25
TRANSVERSAL FILTER
MULTIPLIER LPF
28
DELAY ADJUST
23
26
TRANSVERSAL FILTER
MULTIPLIER LPF
29
DELAY ADJUST
24
RE-SAMPLE DPLL
17
RE-SAMPLE CIRCUIT
18
RE-SAMPLE CIRCUIT
19
14
AGC ATC
15
AGC ATC
16
AGC ATC
11
A/D
12
A/D
13
A/D
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL
10B
HEAD
10A

FIG. 2

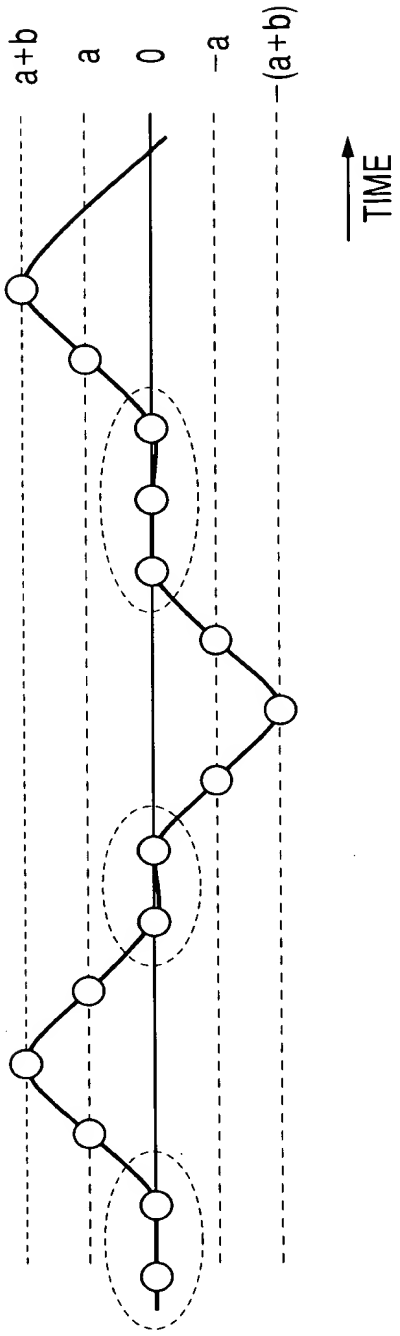


FIG. 3

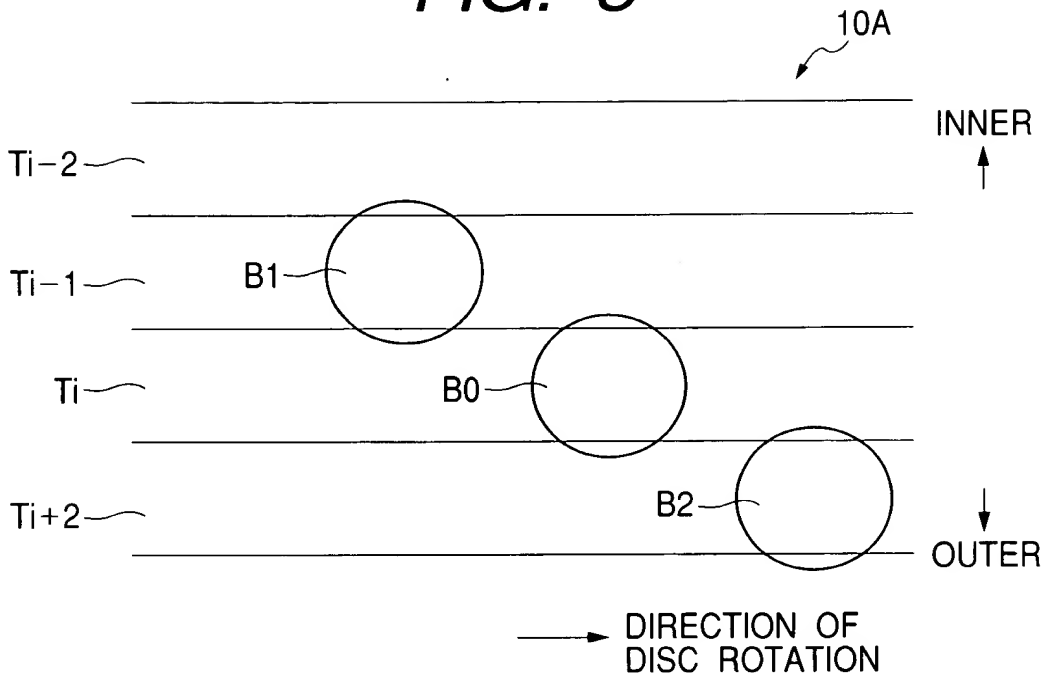

10A
INNER
Ti−2
Ti−1
B1
Ti
B0
Ti+2
B2
OUTER
DIRECTION OF
DISC ROTATION

FIG. 4

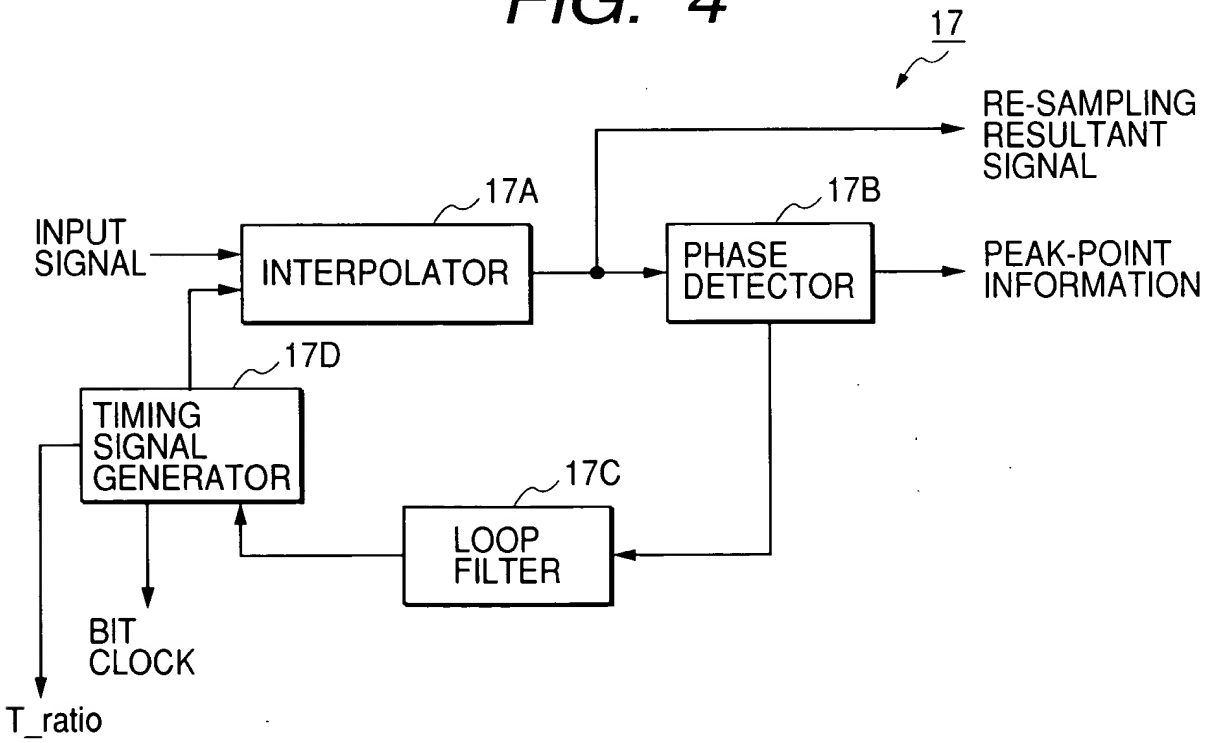

17
RE-SAMPLING
RESULTANT
SIGNAL
17A
17B
INPUT
SIGNAL
INTERPOLATOR
PHASE
DETECTOR
PEAK-POINT
INFORMATION
17D
TIMING
SIGNAL
GENERATOR
17C
LOOP
FILTER
BIT
CLOCK
T_ratio

FIG. 5

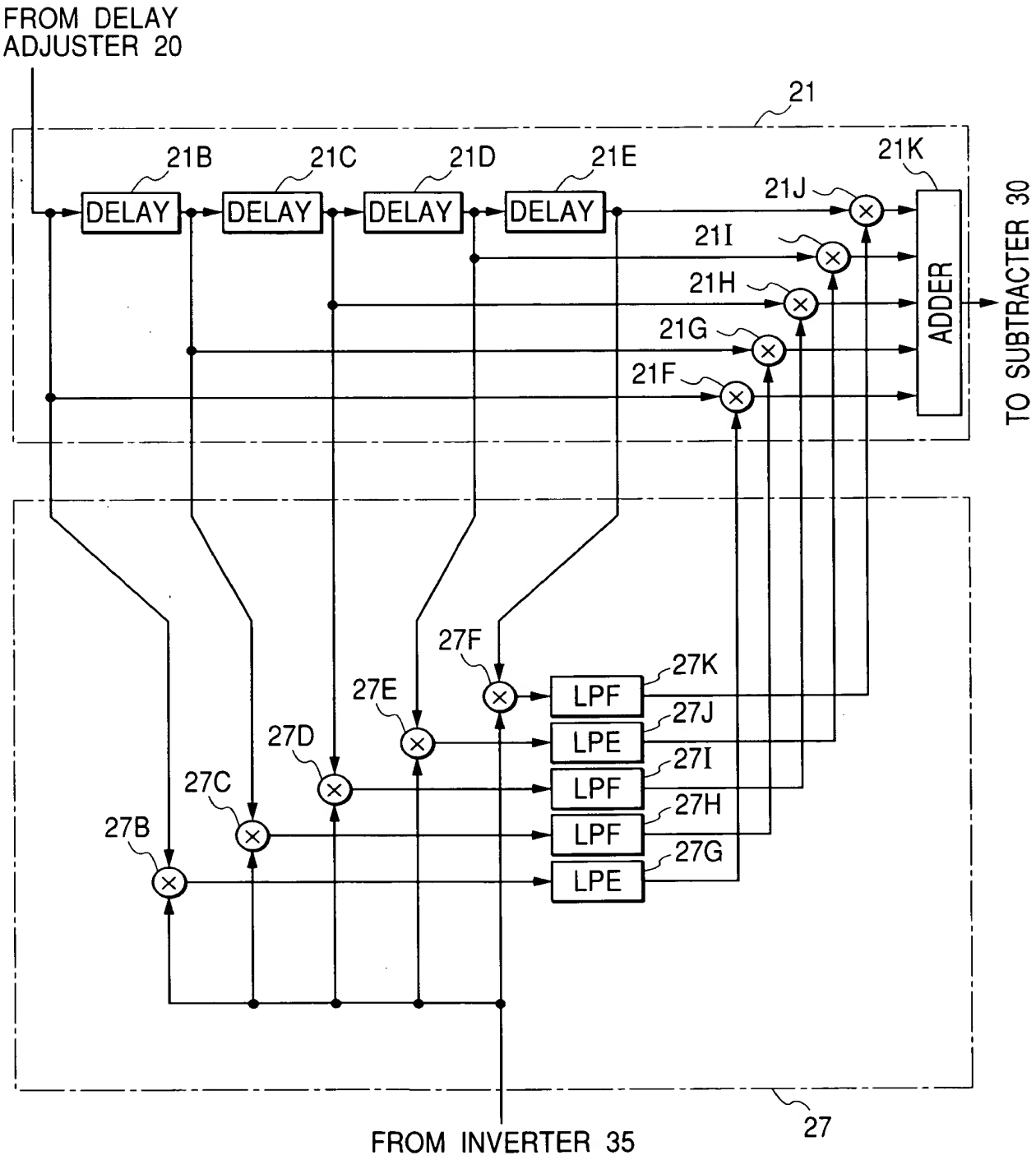

FROM DELAY ADJUSTER 20
21
21B
21C
21D
21E
21K
DELAY
DELAY
DELAY
DELAY
21J
21I
21H
21G
21F
ADDER
TO SUBTRACTER 30
27F
27E
27D
27C
27B
27K
27J
27I
27H
27G
LPF
LPE
LPF
LPF
LPE
FROM INVERTER 35
27

FIG. 6

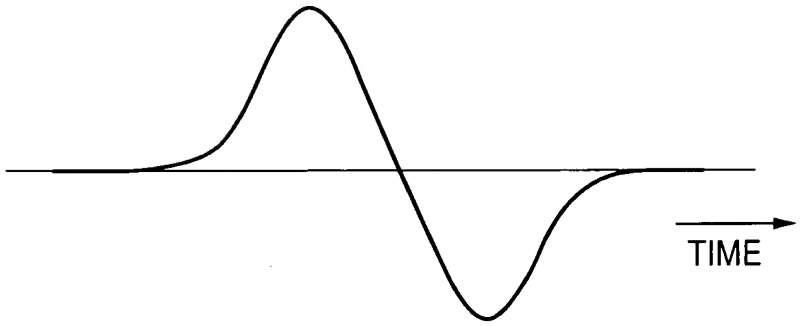


FIG. 7

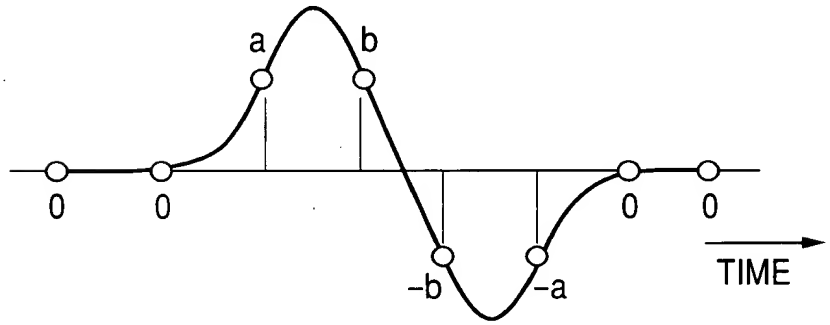
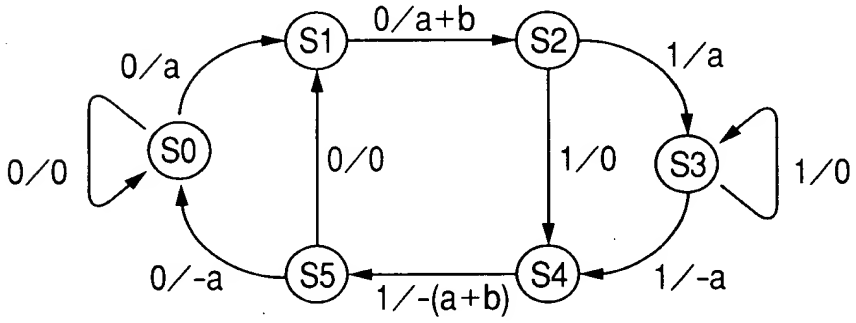
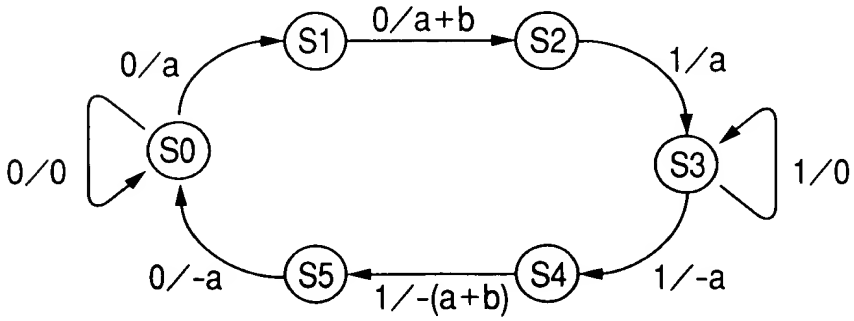


FIG. 8



OUTPUT VALUE/INPUT VALUE

FIG. 9



OUTPUT VALUE/INPUT VALUE

FIG. 10

RLL MODE		RLL (2, X)					
PR MODE		1	2	3	4	5	6
		PR(1, -1)	PR(1,1,-1,-1)	PR(1,2,-2,-1)	PR(1,3,-3,-1)	PR(2,3,-3,-2)	PR(3,4,-4,-3)
TARGET VALUE	a+b	+1	+2	+3	+4	+5	+7
	a	+1	+1	+1	+1	+2	+3
	0	0	0	0	0	0	0
	−a	−1	−1	−1	−1	−2	−3
	−(a+b)	−1	−2	−3	−4	−5	−7
GAIN G		A	A/2	A/3	A/4	A/5	A/7

FIG. 11

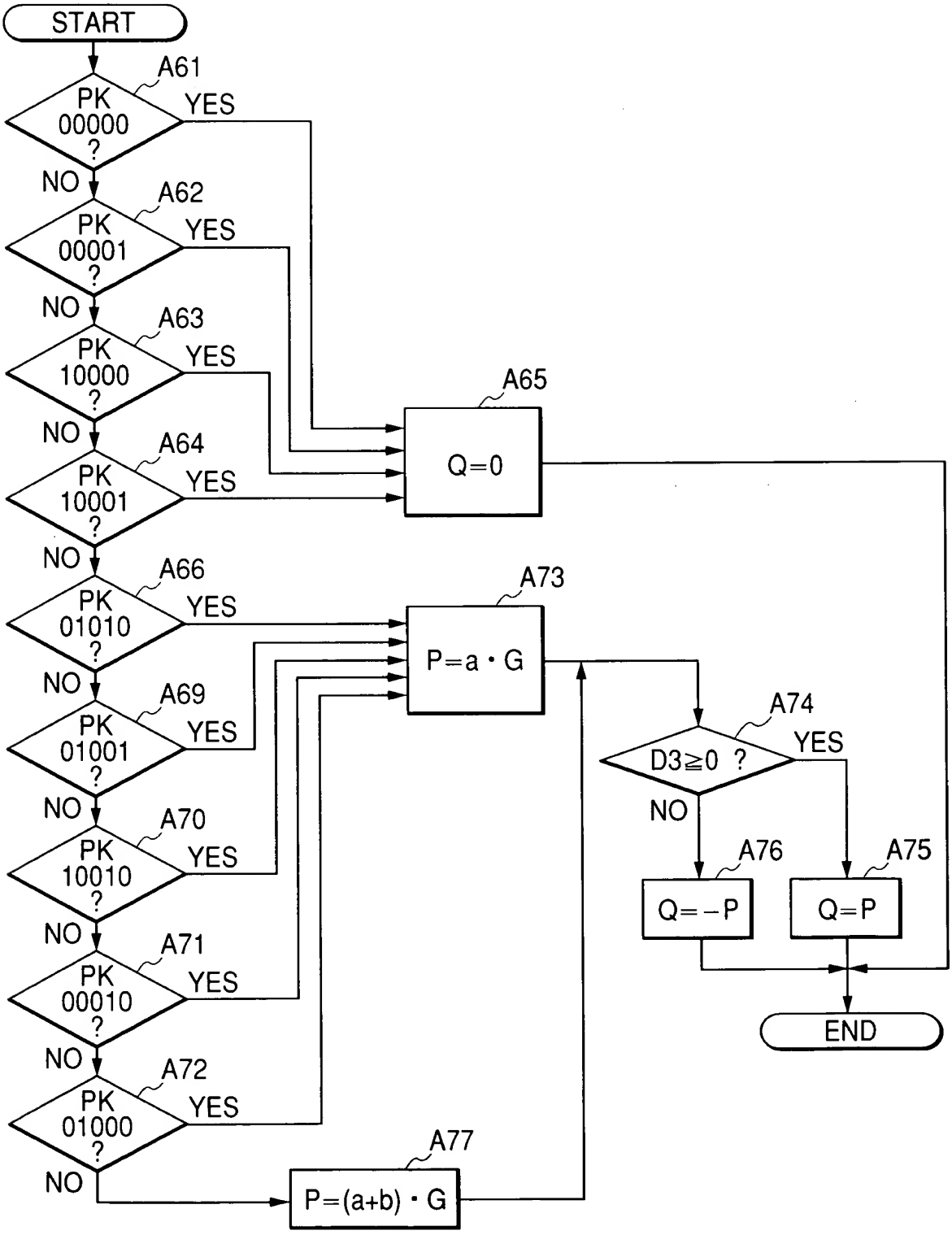

START
A61
PK 00000 ?
YES
NO
A62
PK 00001 ?
YES
NO
A63
PK 10000 ?
YES
NO
A64
PK 10001 ?
YES
NO
A65
Q=0
A66
PK 01010 ?
YES
NO
A69
PK 01001 ?
YES
NO
A70
PK 10010 ?
YES
NO
A71
PK 00010 ?
YES
NO
A72
PK 01000 ?
YES
NO
A73
P=a・G
A74
D3≧0 ?
YES
NO
A75
Q=P
A76
Q=−P
A77
P=(a+b)・G
END

FIG. 12

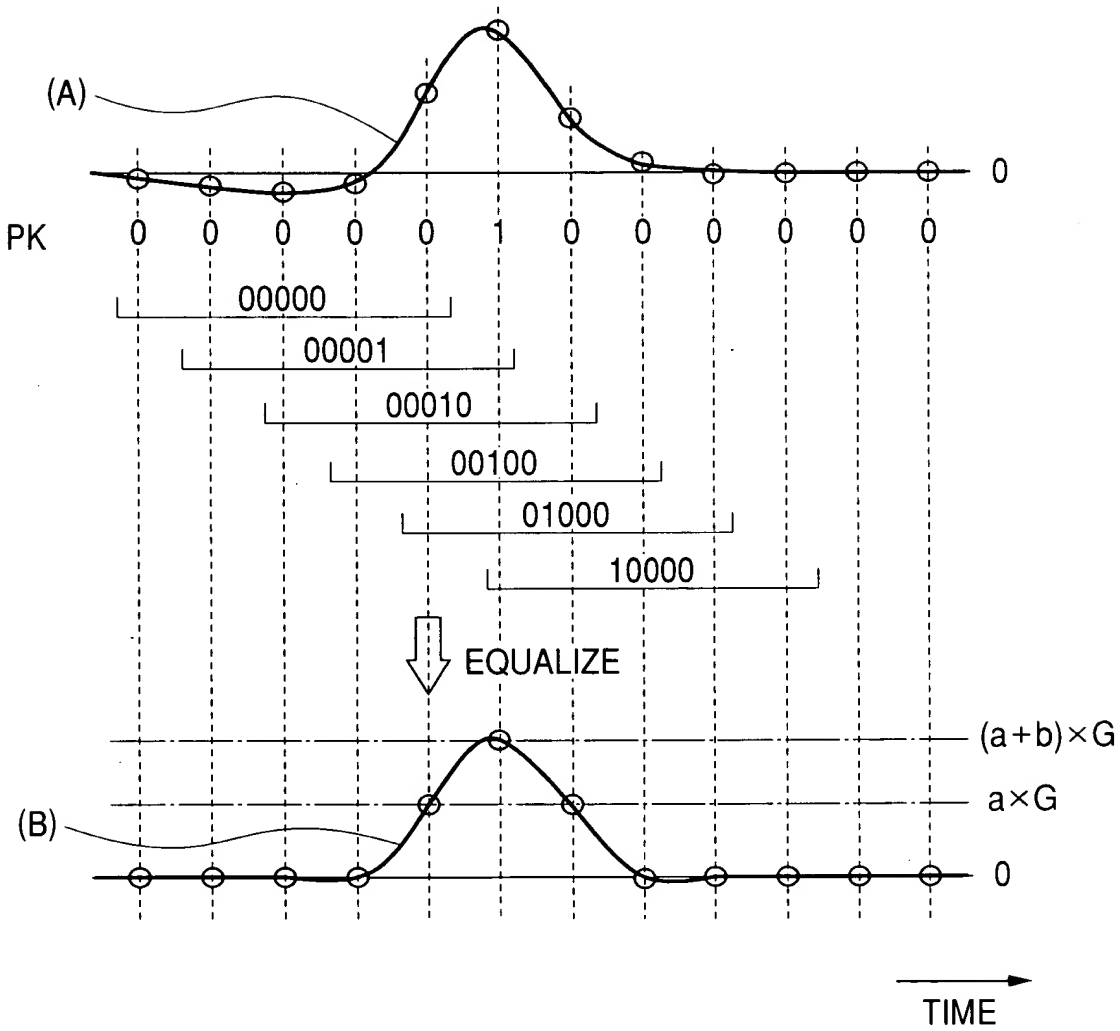

(A)
0
PK
0 0 0 0 0 1 0 0 0 0 0 0
00000
00001
00010
00100
01000
10000
EQUALIZE
(a+b)×G
a×G
(B)
0
TIME

FIG. 13

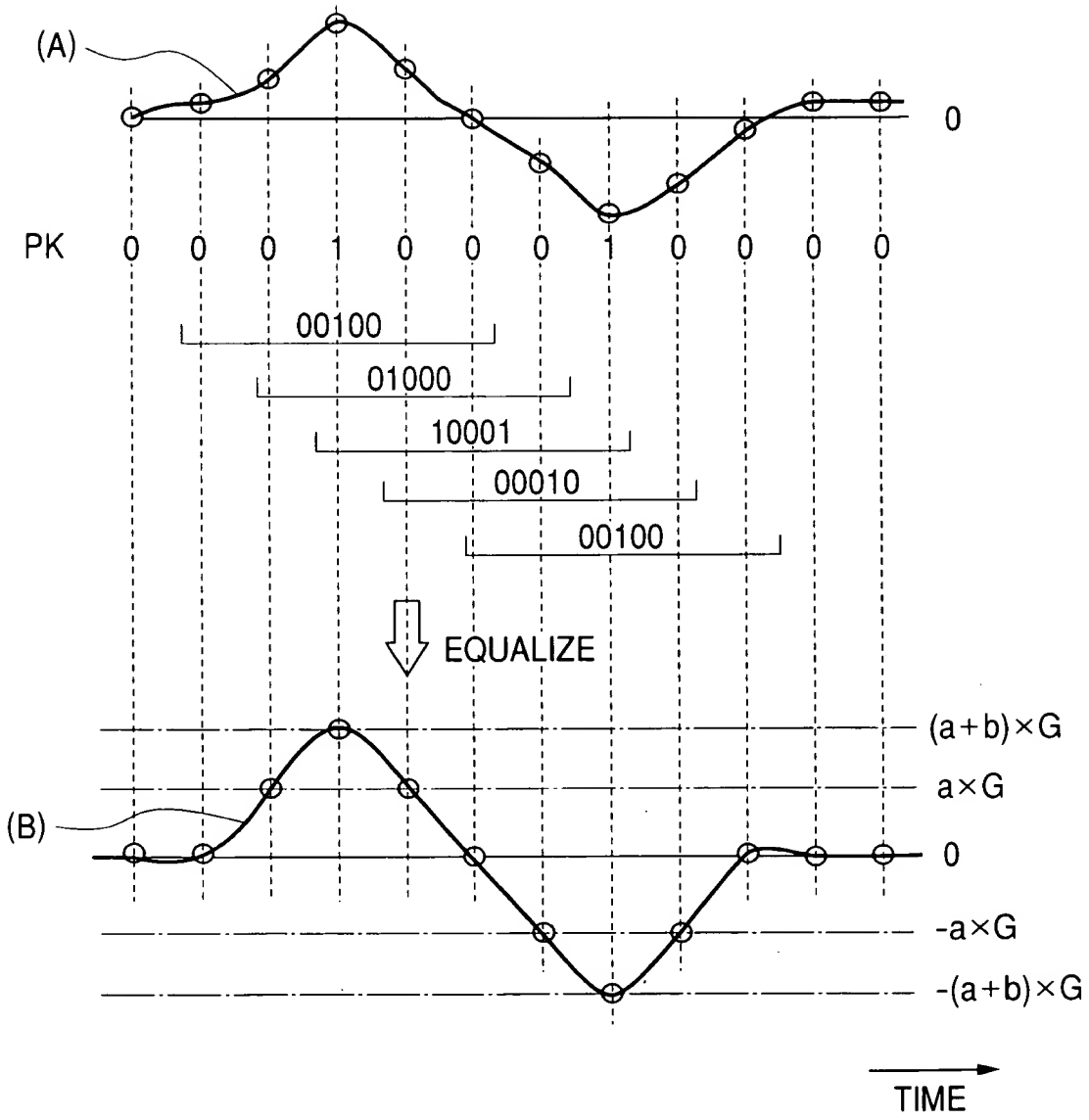

(A)
0
PK
0 0 0 1 0 0 0 1 0 0 0 0
00100
01000
10001
00010
00100
EQUALIZE
(a+b)×G
a×G
(B)
0
-a×G
-(a+b)×G
TIME

FIG. 14

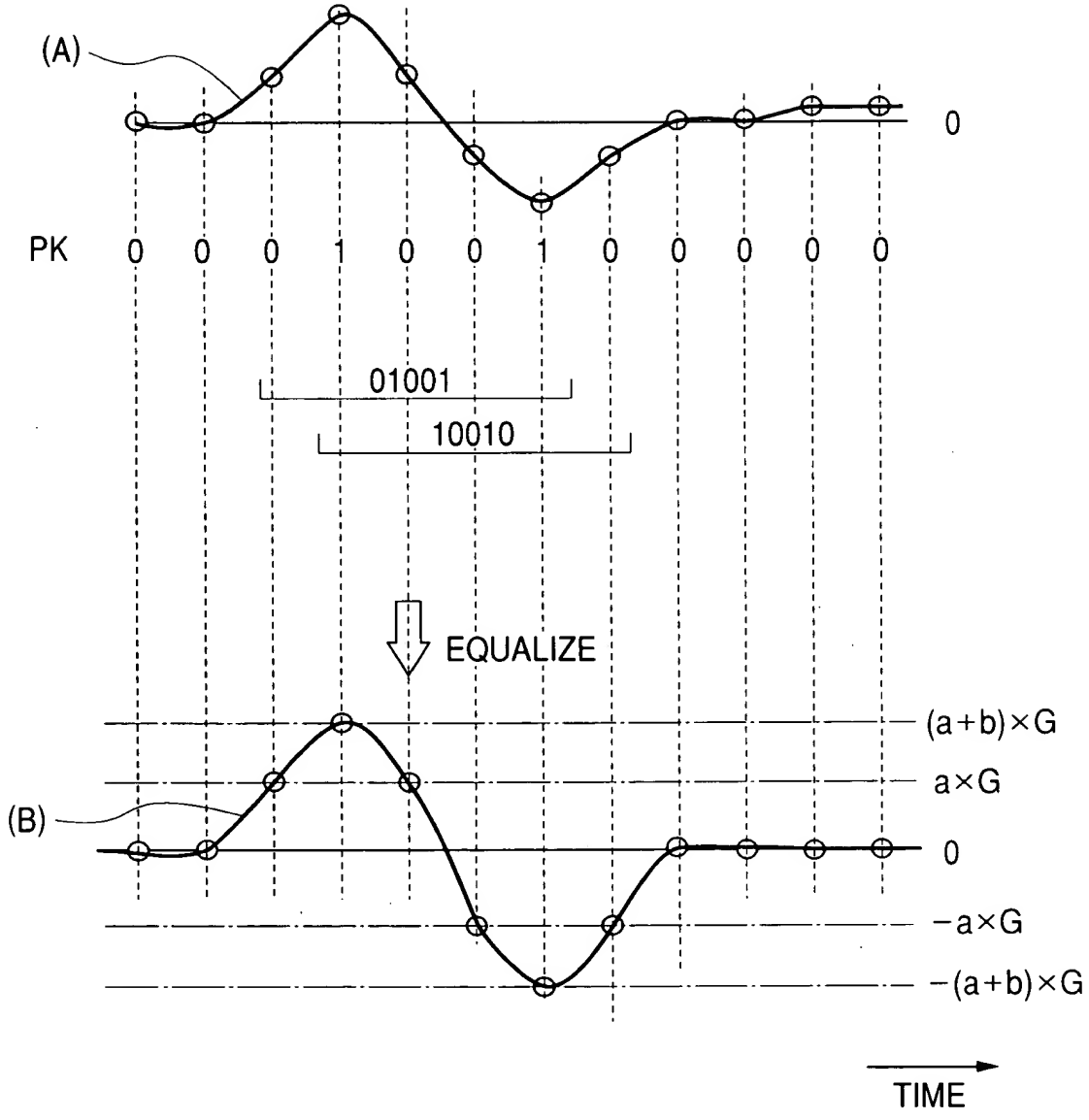

(A)
0
PK
0 0 0 1 0 0 1 0 0 0 0 0
01001
10010
EQUALIZE
(a+b)×G
a×G
(B)
0
−a×G
−(a+b)×G
TIME

FIG. 15

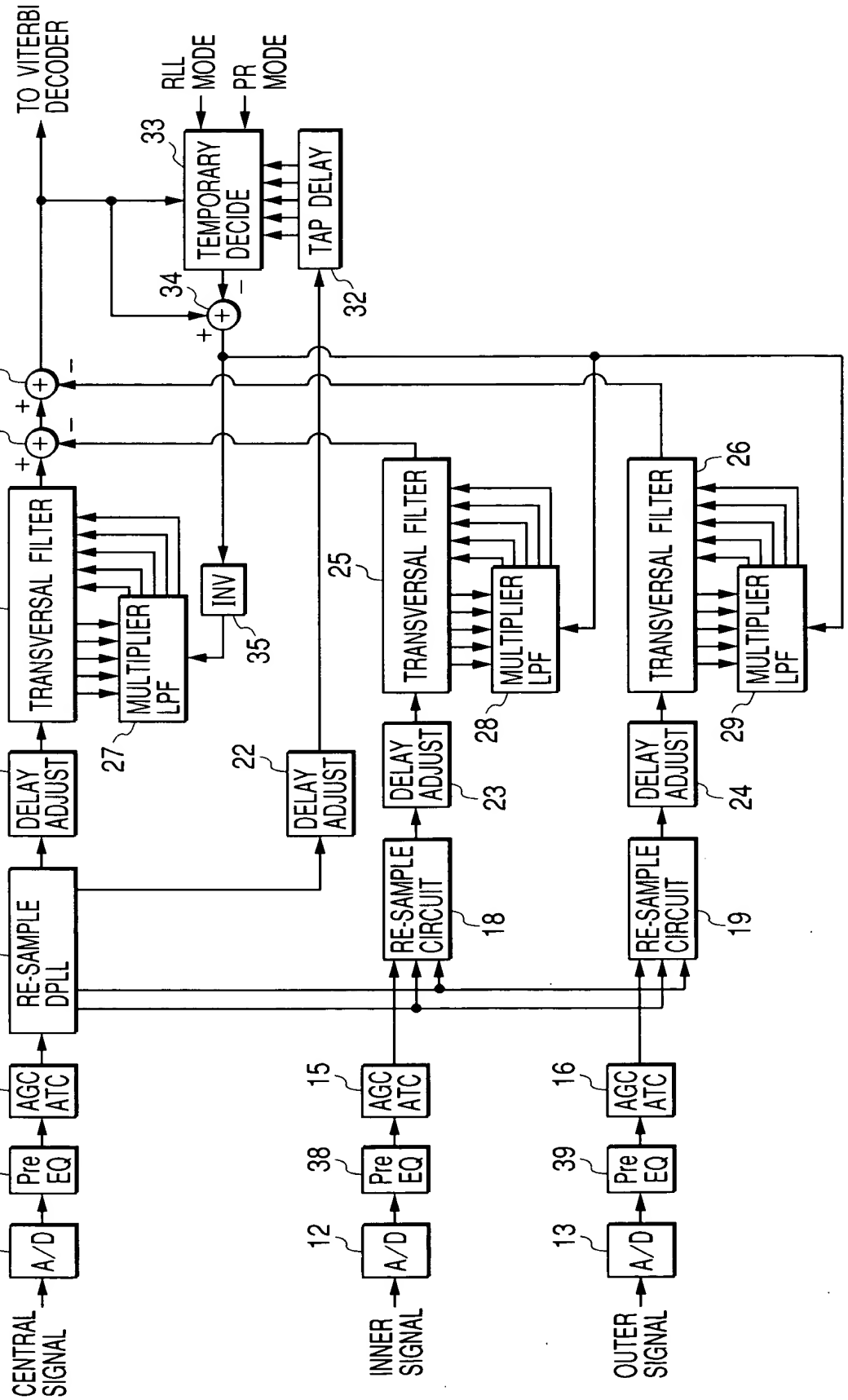

CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL
A/D
Pre EQ
AGC ATC
RE-SAMPLE DPLL
RE-SAMPLE CIRCUIT
DELAY ADJUST
TRANSVERSAL FILTER
MULTIPLIER LPF
INV
TEMPORARY DECIDE
TAP DELAY
RLL MODE
PR MODE
TO VITERBI DECODER
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
37
38
39

FIG. 16

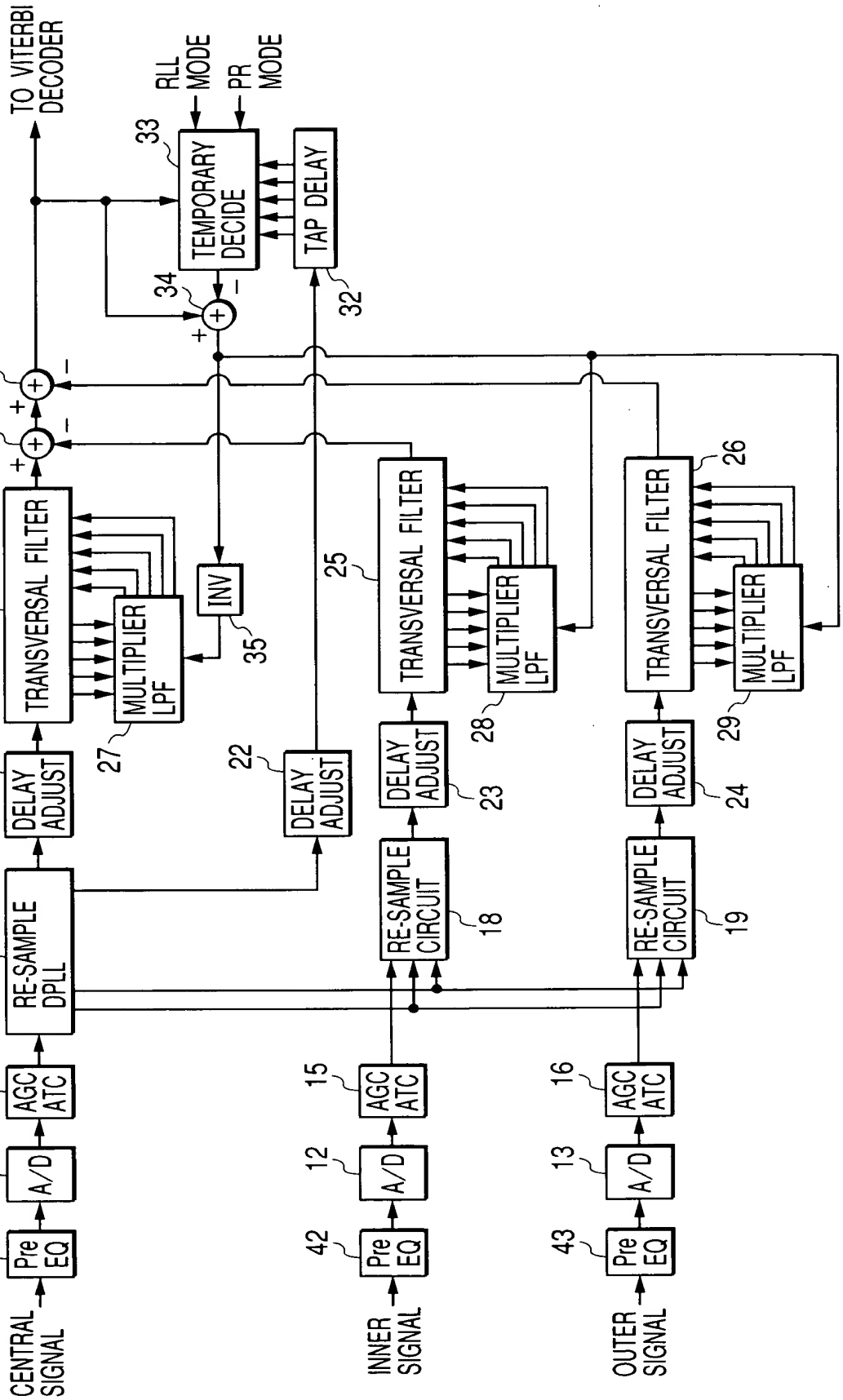

TO VITERBI DECODER
RLL MODE
PR MODE
33
TEMPORARY DECIDE
TAP DELAY
32
34
31
30
TRANSVERSAL FILTER
21
MULTIPLIER LPF
27
INV
35
25
TRANSVERSAL FILTER
MULTIPLIER LPF
28
26
TRANSVERSAL FILTER
MULTIPLIER LPF
29
20
DELAY ADJUST
22
DELAY ADJUST
23
DELAY ADJUST
24
17
RE-SAMPLE DPLL
RE-SAMPLE CIRCUIT
18
RE-SAMPLE CIRCUIT
19
14
AGC ATC
15
AGC ATC
16
AGC ATC
11
A/D
12
A/D
13
A/D
41
Pre EQ
42
Pre EQ
43
Pre EQ
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL

FIG. 17

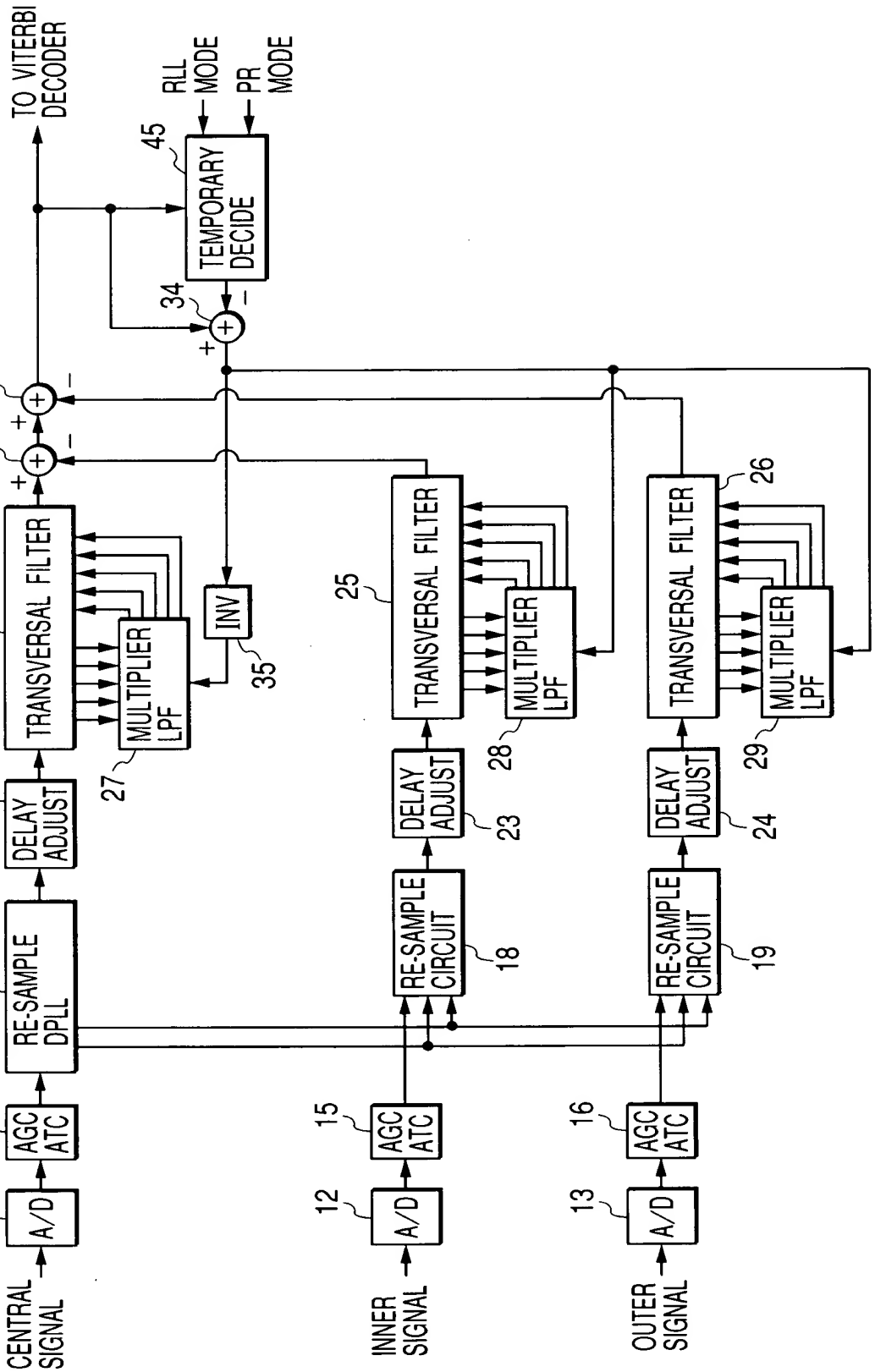

CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL
A/D
AGC ATC
RE-SAMPLE DPLL
RE-SAMPLE CIRCUIT
DELAY ADJUST
TRANSVERSAL FILTER
MULTIPLIER LPF
INV
TEMPORARY DECIDE
RLL MODE
PR MODE
TO VITERBI DECODER
11
12
13
14
15
16
17
18
19
20
21
23
24
25
26
27
28
29
30
31
34
35
45

FIG. 18

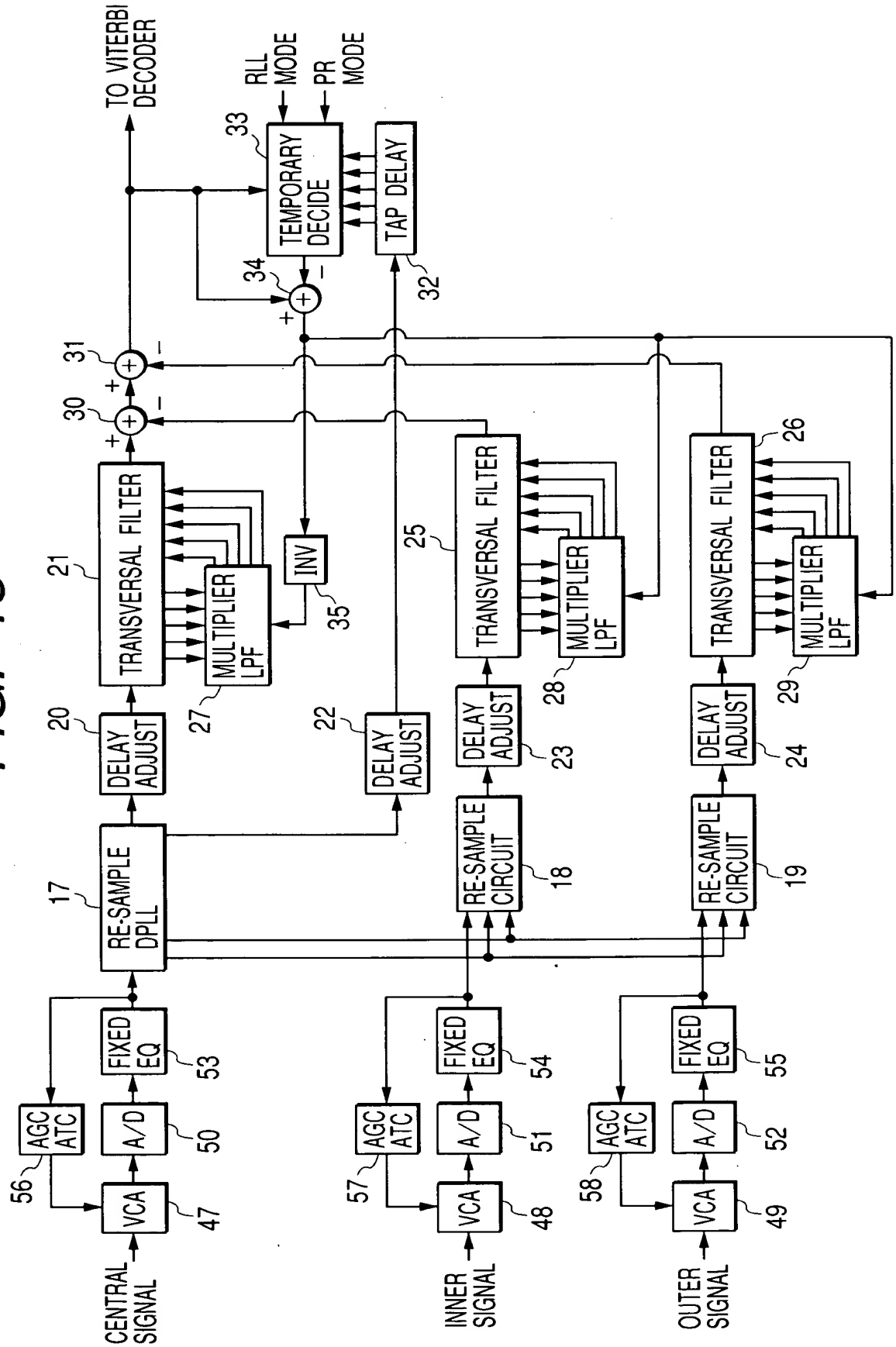

TO VITERBI DECODER
RLL MODE
PR MODE
33
TEMPORARY DECIDE
TAP DELAY
34
32
31
30
TRANSVERSAL FILTER
21
MULTIPLIER LPF
27
INV
35
DELAY ADJUST
20
22
RE-SAMPLE DPLL
17
25
TRANSVERSAL FILTER
MULTIPLIER LPF
28
DELAY ADJUST
23
RE-SAMPLE CIRCUIT
18
26
TRANSVERSAL FILTER
MULTIPLIER LPF
29
DELAY ADJUST
24
RE-SAMPLE CIRCUIT
19
FIXED EQ
53
54
55
A/D
50
51
52
AGC ATC
56
57
58
VCA
47
48
49
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL

FIG. 19

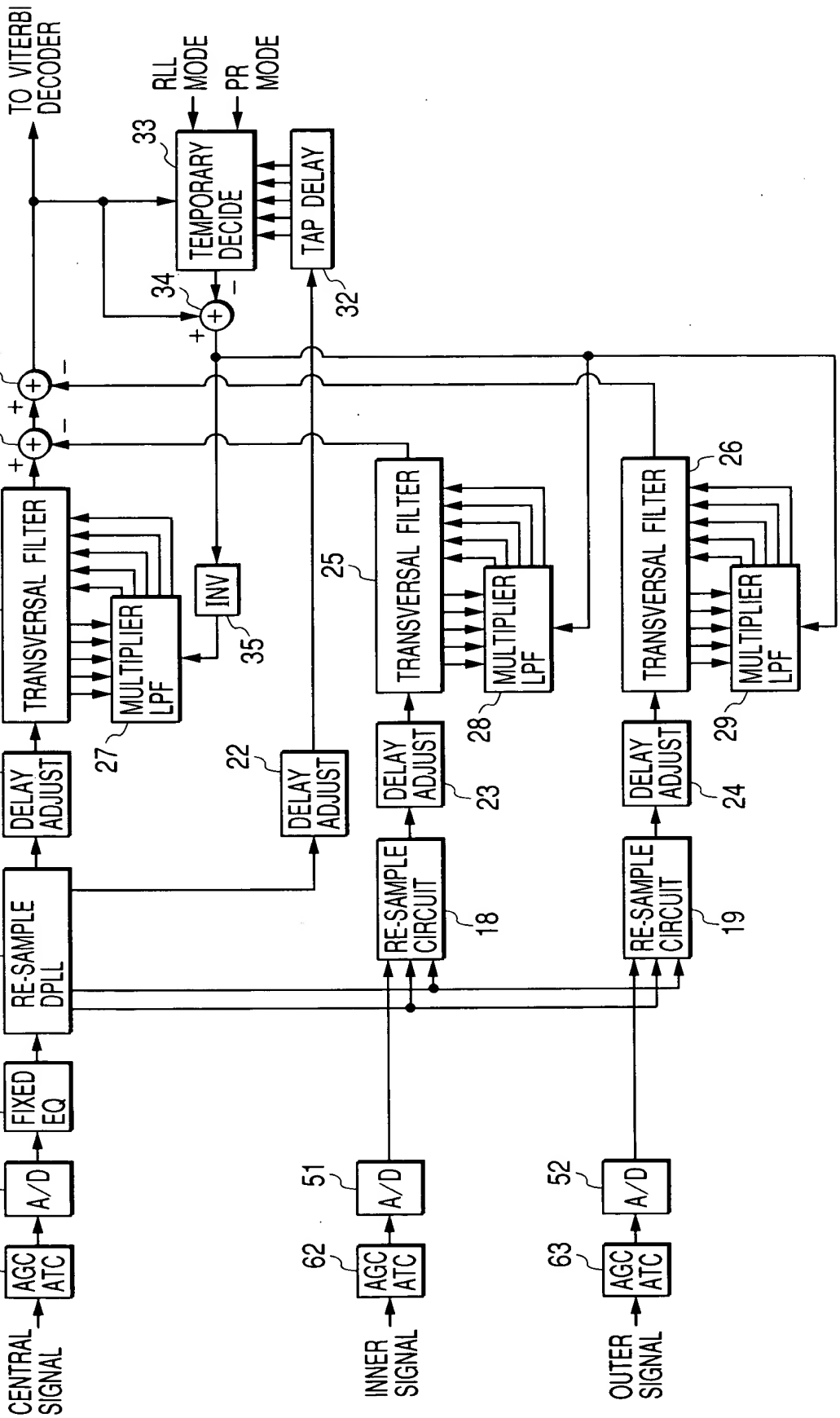

CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL
AGC ATC
A/D
FIXED EQ
RE-SAMPLE DPLL
RE-SAMPLE CIRCUIT
DELAY ADJUST
TRANSVERSAL FILTER
MULTIPLIER LPF
INV
TEMPORARY DECIDE
TAP DELAY
RLL MODE
PR MODE
TO VITERBI DECODER
61
62
63
50
51
52
53
17
18
19
20
22
23
24
21
25
26
27
28
29
30
31
33
34
35
32

FIG. 20

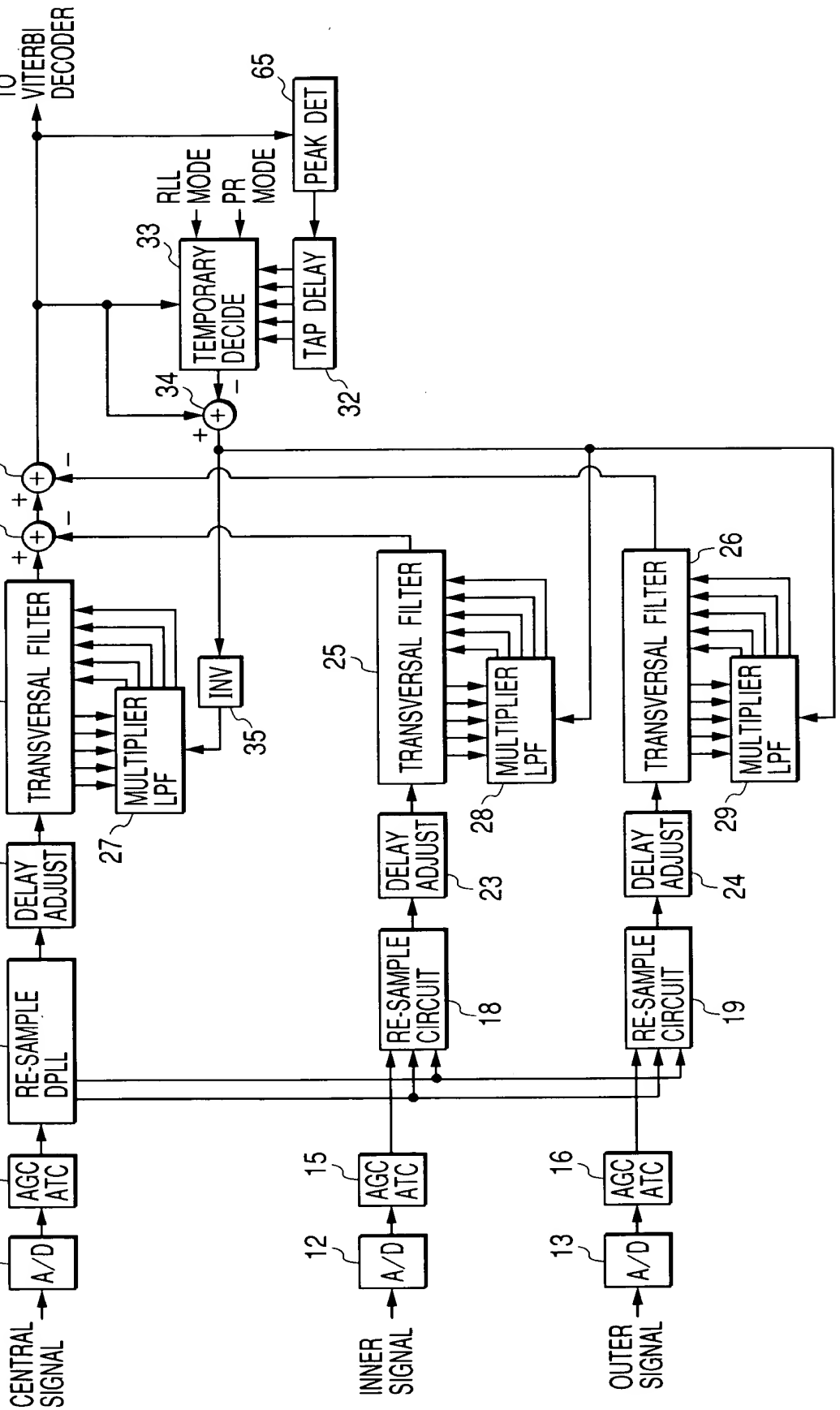

CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL
A/D
AGC ATC
RE-SAMPLE DPLL
RE-SAMPLE CIRCUIT
DELAY ADJUST
TRANSVERSAL FILTER
TRANSVERSAL FILTER
TRANSVERSAL FILTER
MULTIPLIER LPF
MULTIPLIER LPF
MULTIPLIER LPF
INV
TEMPORARY DECIDE
TAP DELAY
PEAK DET
RLL MODE
PR MODE
TO VITERBI DECODER
11
12
13
14
15
16
17
18
19
20
21
23
24
25
26
27
28
29
30
31
32
33
34
35
65

FIG. 21

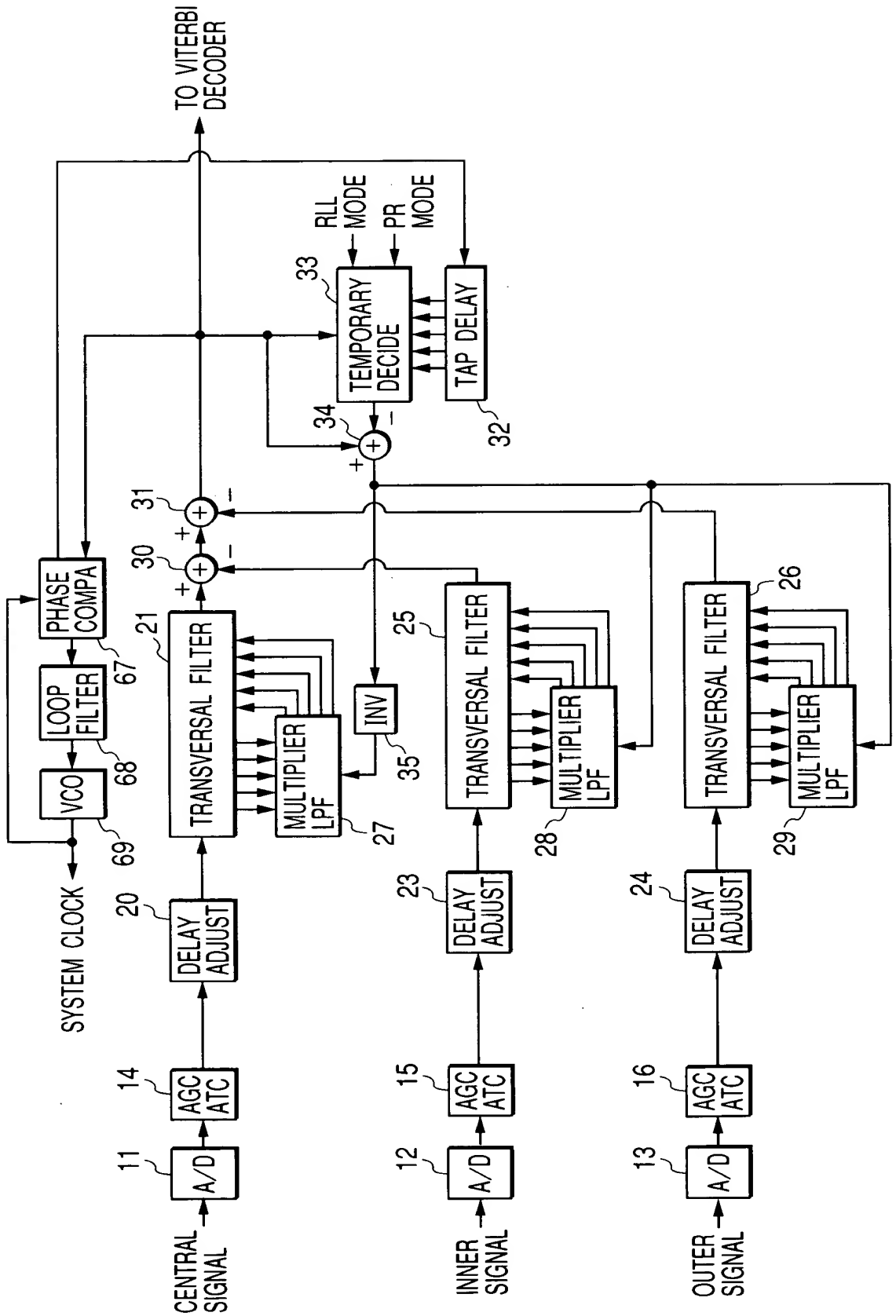

TO VITERBI DECODER
RLL MODE
PR MODE
33
TEMPORARY DECIDE
TAP DELAY
32
34
31
30
PHASE COMPA
67
LOOP FILTER
68
VCO
69
SYSTEM CLOCK
21
TRANSVERSAL FILTER
MULTIPLIER LPF
27
INV
35
25
TRANSVERSAL FILTER
MULTIPLIER LPF
28
26
TRANSVERSAL FILTER
MULTIPLIER LPF
29
20
DELAY ADJUST
23
DELAY ADJUST
24
DELAY ADJUST
14
AGC ATC
15
AGC ATC
16
AGC ATC
11
A/D
12
A/D
13
A/D
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL

FIG. 22

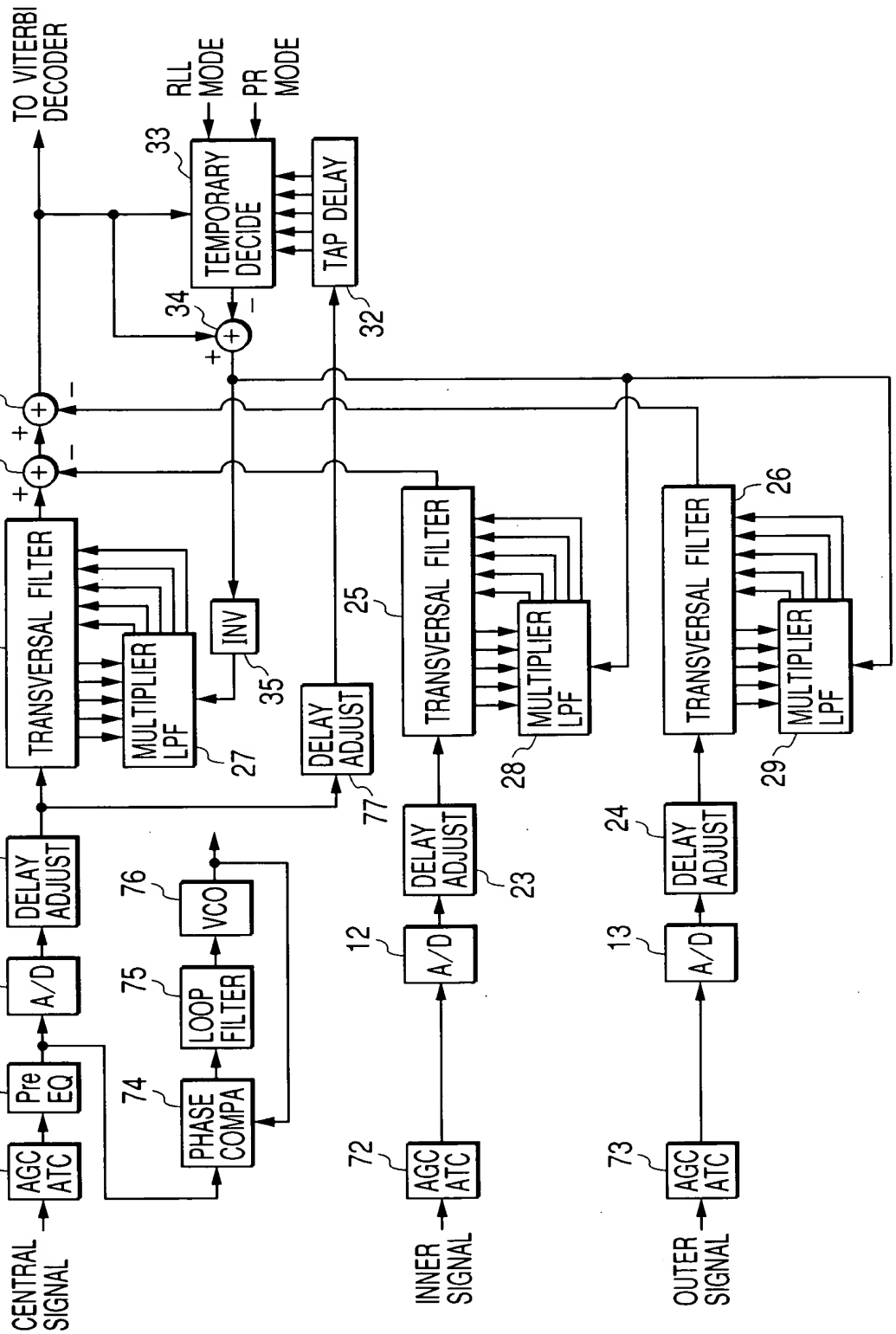

CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL
AGC ATC
Pre EQ
A/D
DELAY ADJUST
PHASE COMPA
LOOP FILTER
VCO
TRANSVERSAL FILTER
MULTIPLIER LPF
INV
TEMPORARY DECIDE
TAP DELAY
RLL MODE
PR MODE
TO VITERBI DECODER
71
72
73
74
75
76
41
11
12
13
20
21
23
24
25
26
27
28
29
30
31
32
33
34
35
77

FIG. 23

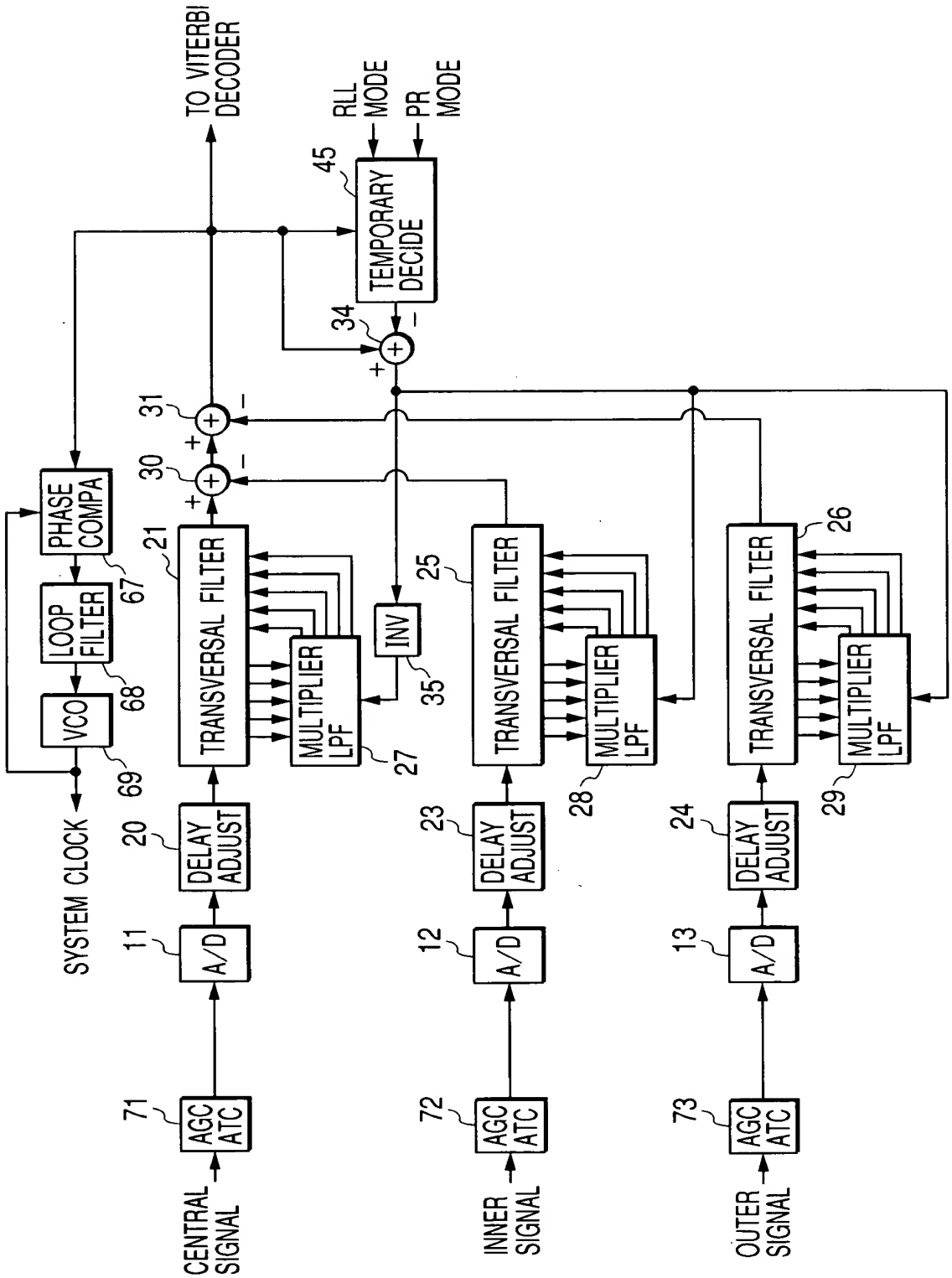

TO VITERBI DECODER
RLL MODE
PR MODE
45
TEMPORARY DECIDE
34
31
30
PHASE COMPA
67
LOOP FILTER
68
VCO
69
SYSTEM CLOCK
21
TRANSVERSAL FILTER
MULTIPLIER LPF
27
INV
35
25
TRANSVERSAL FILTER
MULTIPLIER LPF
28
26
TRANSVERSAL FILTER
MULTIPLIER LPF
29
20
DELAY ADJUST
23
DELAY ADJUST
24
DELAY ADJUST
11
A/D
12
A/D
13
A/D
71
AGC ATC
72
AGC ATC
73
AGC ATC
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL

FIG. 24

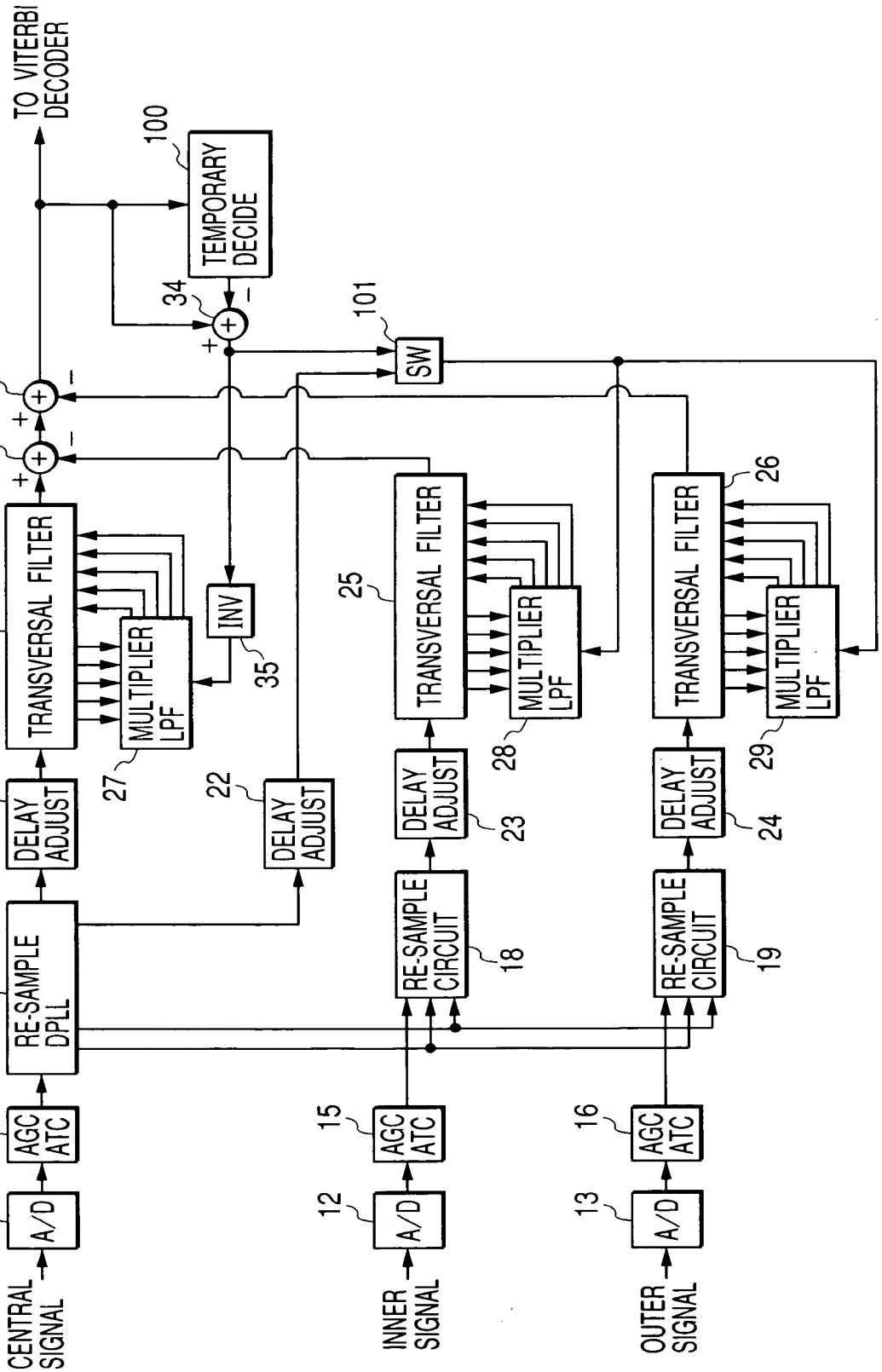

CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL
A/D
AGC ATC
RE-SAMPLE DPLL
RE-SAMPLE CIRCUIT
DELAY ADJUST
TRANSVERSAL FILTER
MULTIPLIER LPF
INV
TEMPORARY DECIDE
SW
TO VITERBI DECODER
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
34
35
100
101

FIG. 25

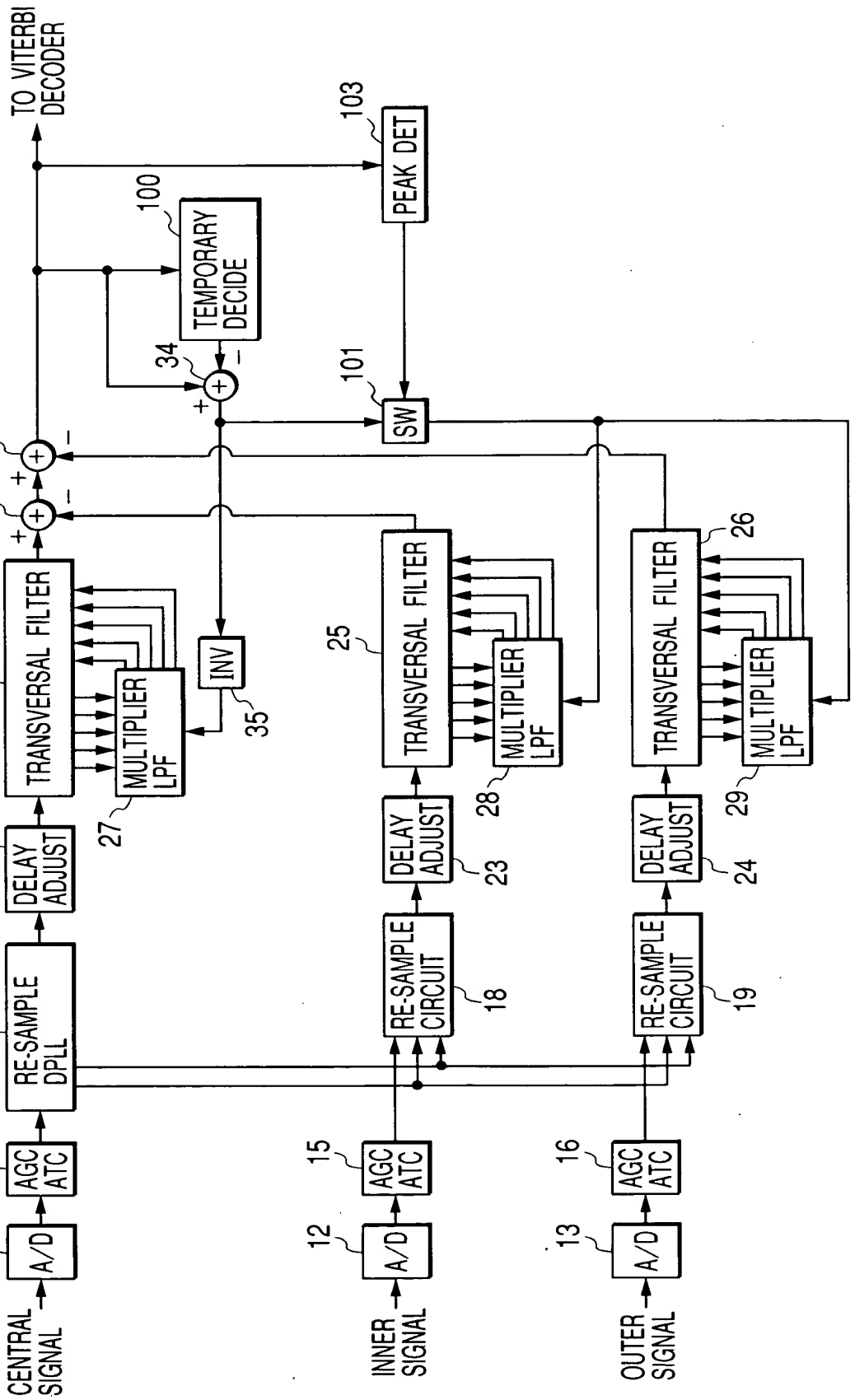

CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL
A/D
AGC ATC
RE-SAMPLE DPLL
RE-SAMPLE CIRCUIT
DELAY ADJUST
TRANSVERSAL FILTER
TRANSVERSAL FILTER
TRANSVERSAL FILTER
MULTIPLIER LPF
MULTIPLIER LPF
MULTIPLIER LPF
INV
SW
PEAK DET
TEMPORARY DECIDE
TO VITERBI DECODER
11
12
13
14
15
16
17
18
19
20
21
23
24
25
26
27
28
29
30
31
34
35
100
101
103

FIG. 26

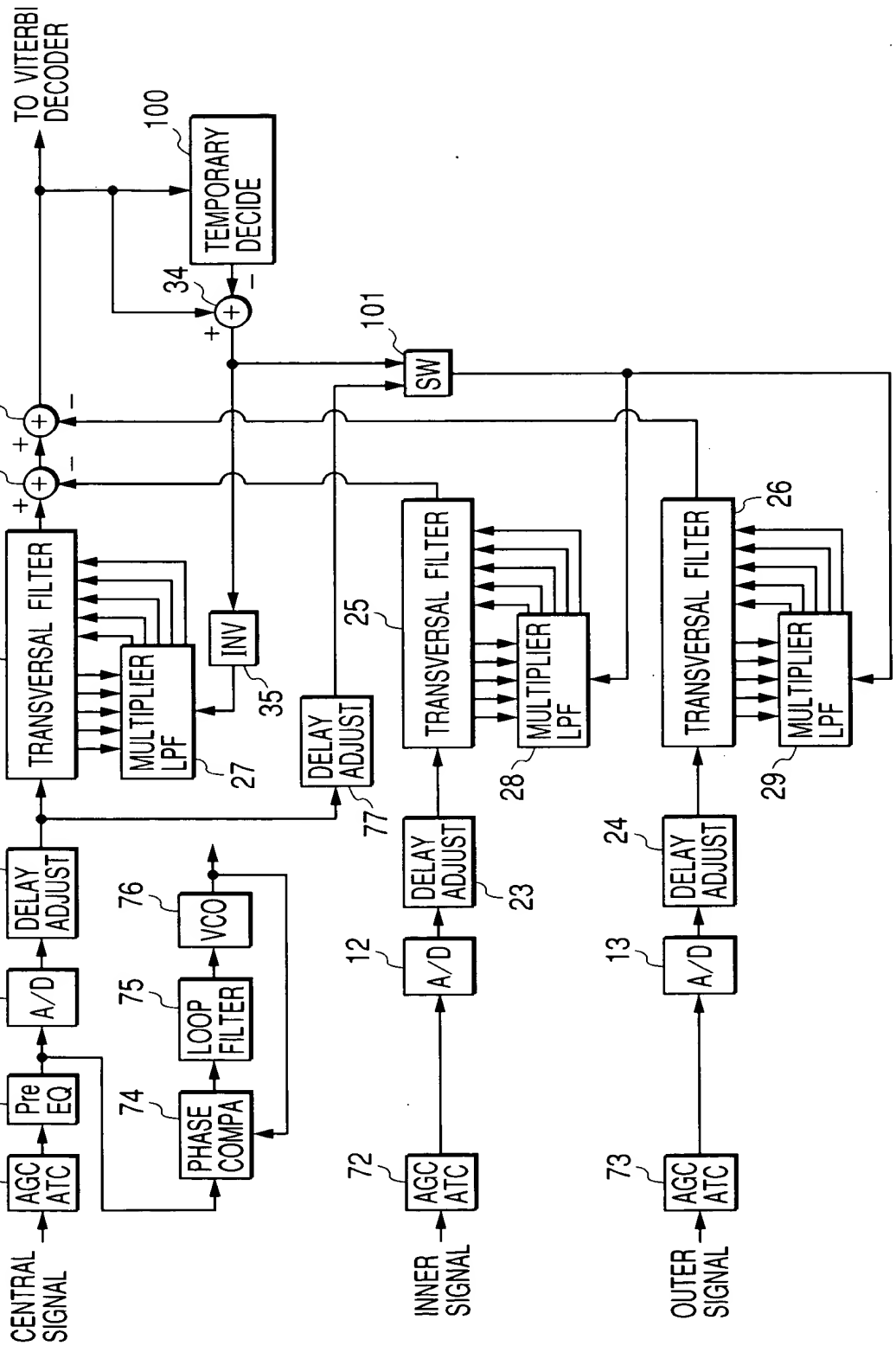

TO VITERBI DECODER
100
TEMPORARY DECIDE
34
101
SW
31
30
21
TRANSVERSAL FILTER
MULTIPLIER LPF
27
INV
35
DELAY ADJUST
77
25
TRANSVERSAL FILTER
MULTIPLIER LPF
28
26
TRANSVERSAL FILTER
MULTIPLIER LPF
29
20
DELAY ADJUST
11
A/D
41
Pre EQ
71
AGC ATC
CENTRAL SIGNAL
76
VCO
75
LOOP FILTER
74
PHASE COMPA
DELAY ADJUST
23
12
A/D
72
AGC ATC
INNER SIGNAL
DELAY ADJUST
24
13
A/D
73
AGC ATC
OUTER SIGNAL

FIG. 27

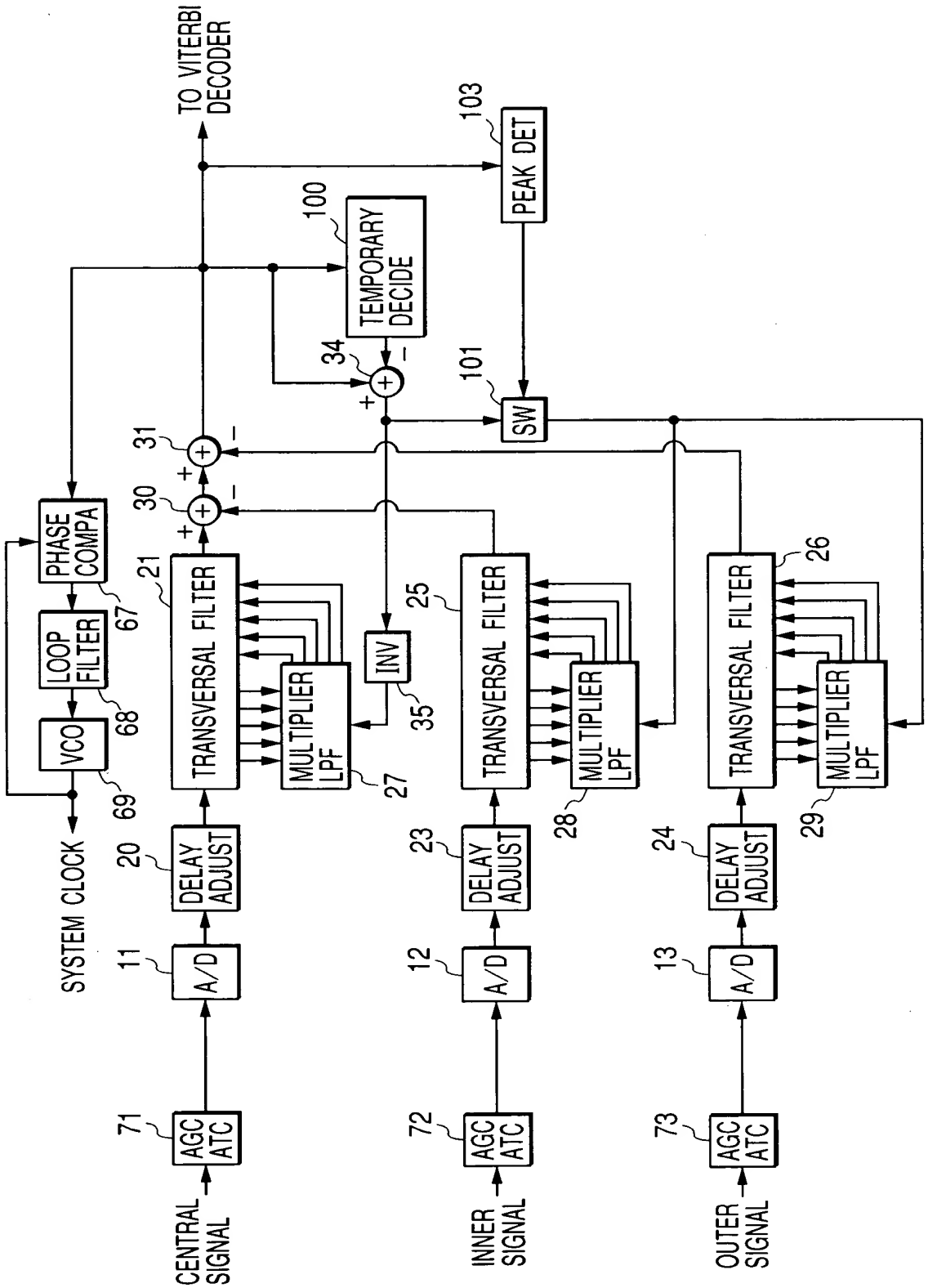

TO VITERBI DECODER
PEAK DET
103
TEMPORARY DECIDE
100
34
101
SW
31
30
PHASE COMPA
LOOP FILTER
VCO
67
68
69
SYSTEM CLOCK
21
TRANSVERSAL FILTER
MULTIPLIER LPF
27
INV
35
25
TRANSVERSAL FILTER
MULTIPLIER LPF
28
26
TRANSVERSAL FILTER
MULTIPLIER LPF
29
20
DELAY ADJUST
23
DELAY ADJUST
24
DELAY ADJUST
11
A/D
12
A/D
13
A/D
71
AGC ATC
72
AGC ATC
73
AGC ATC
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL

FIG. 28

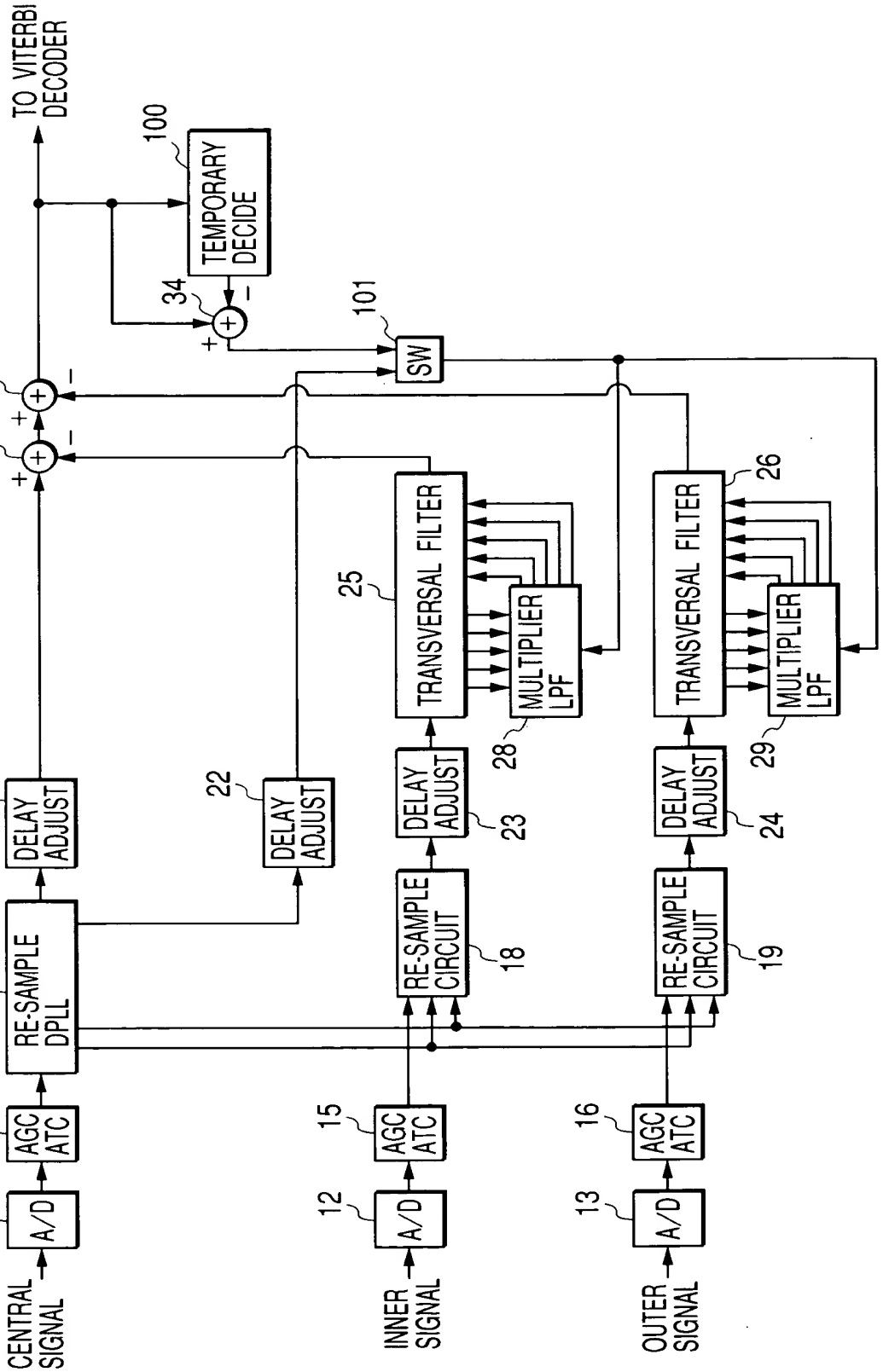

CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL
A/D
AGC ATC
RE-SAMPLE DPLL
RE-SAMPLE CIRCUIT
DELAY ADJUST
TRANSVERSAL FILTER
MULTIPLIER LPF
TEMPORARY DECIDE
SW
TO VITERBI DECODER
11
12
13
14
15
16
17
18
19
20
22
23
24
25
26
28
29
30
31
34
100
101

FIG. 29

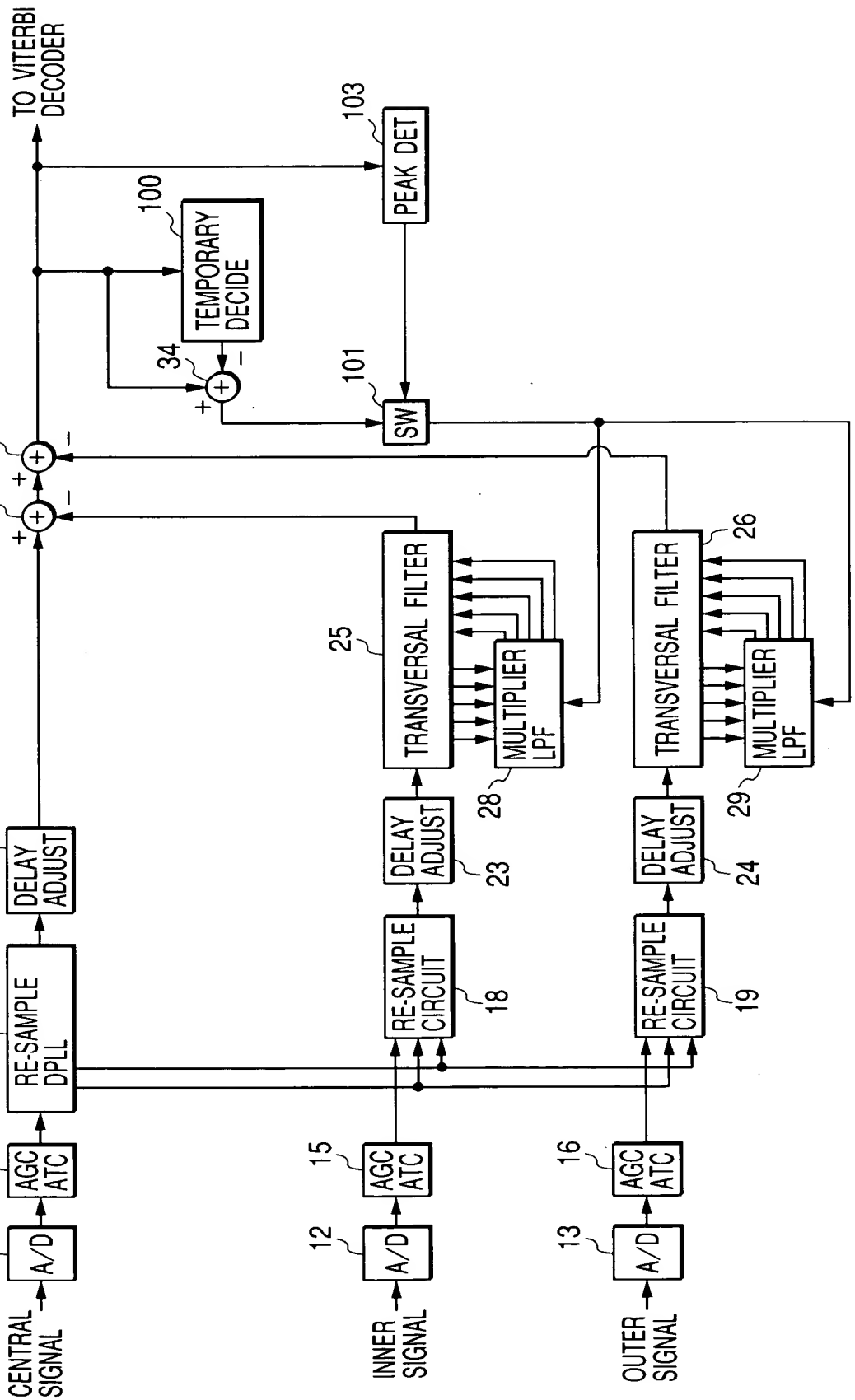

TO VITERBI DECODER
103
PEAK DET
100
TEMPORARY DECIDE
34
101
SW
31
30
25
TRANSVERSAL FILTER
MULTIPLIER LPF
28
26
TRANSVERSAL FILTER
MULTIPLIER LPF
29
20
DELAY ADJUST
23
DELAY ADJUST
24
17
RE-SAMPLE DPLL
18
RE-SAMPLE CIRCUIT
19
RE-SAMPLE CIRCUIT
14
AGC ATC
15
AGC ATC
16
AGC ATC
11
A/D
12
A/D
13
A/D
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL

FIG. 30

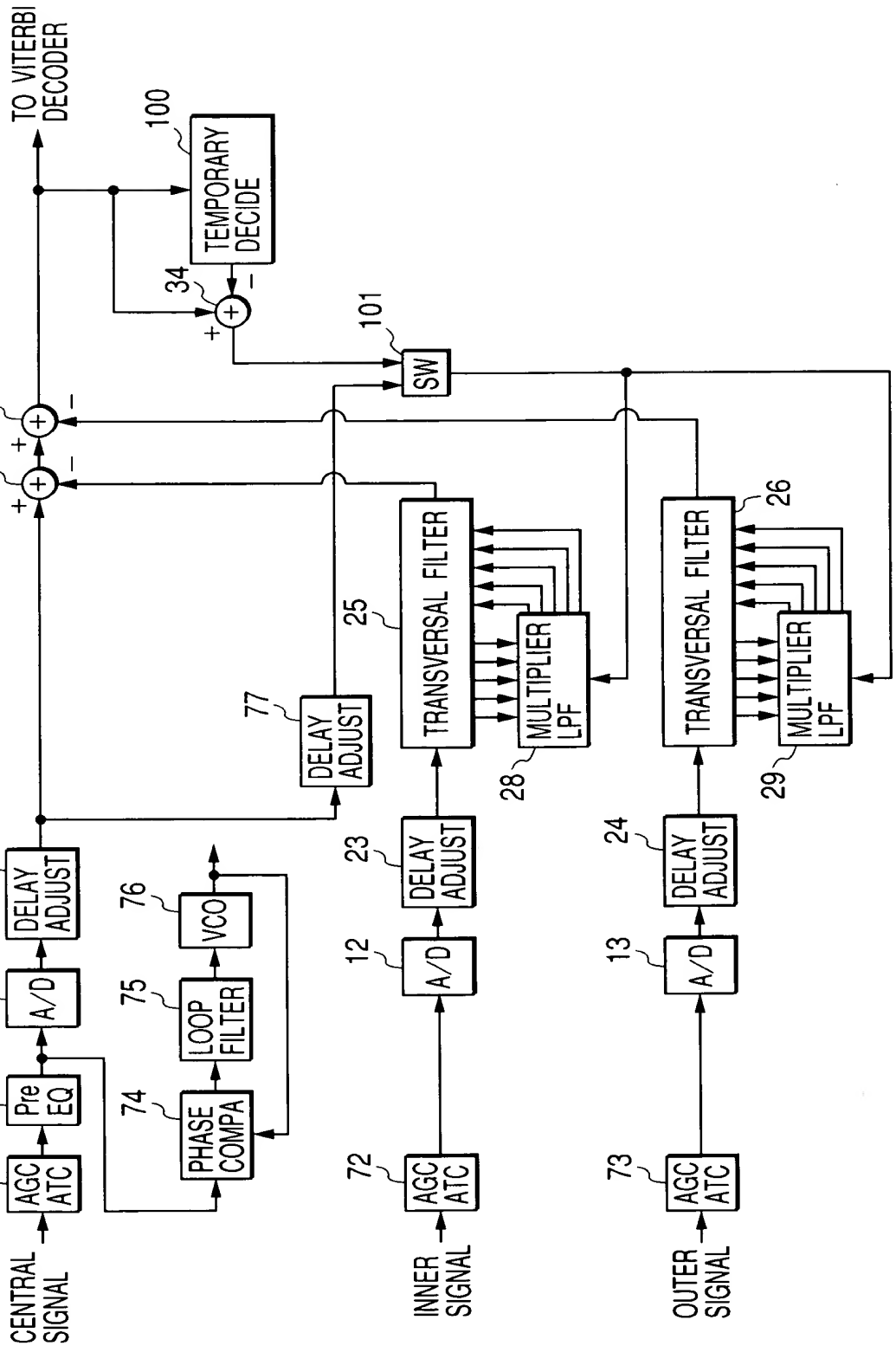

TO VITERBI DECODER
100
TEMPORARY DECIDE
34
101
SW
31
30
77
DELAY ADJUST
25
TRANSVERSAL FILTER
MULTIPLIER LPF
28
26
29
20
DELAY ADJUST
11
A/D
41
Pre EQ
71
AGC ATC
CENTRAL SIGNAL
74
PHASE COMPA
75
LOOP FILTER
76
VCO
23
DELAY ADJUST
12
A/D
72
AGC ATC
INNER SIGNAL
24
DELAY ADJUST
13
A/D
73
AGC ATC
OUTER SIGNAL

FIG. 31

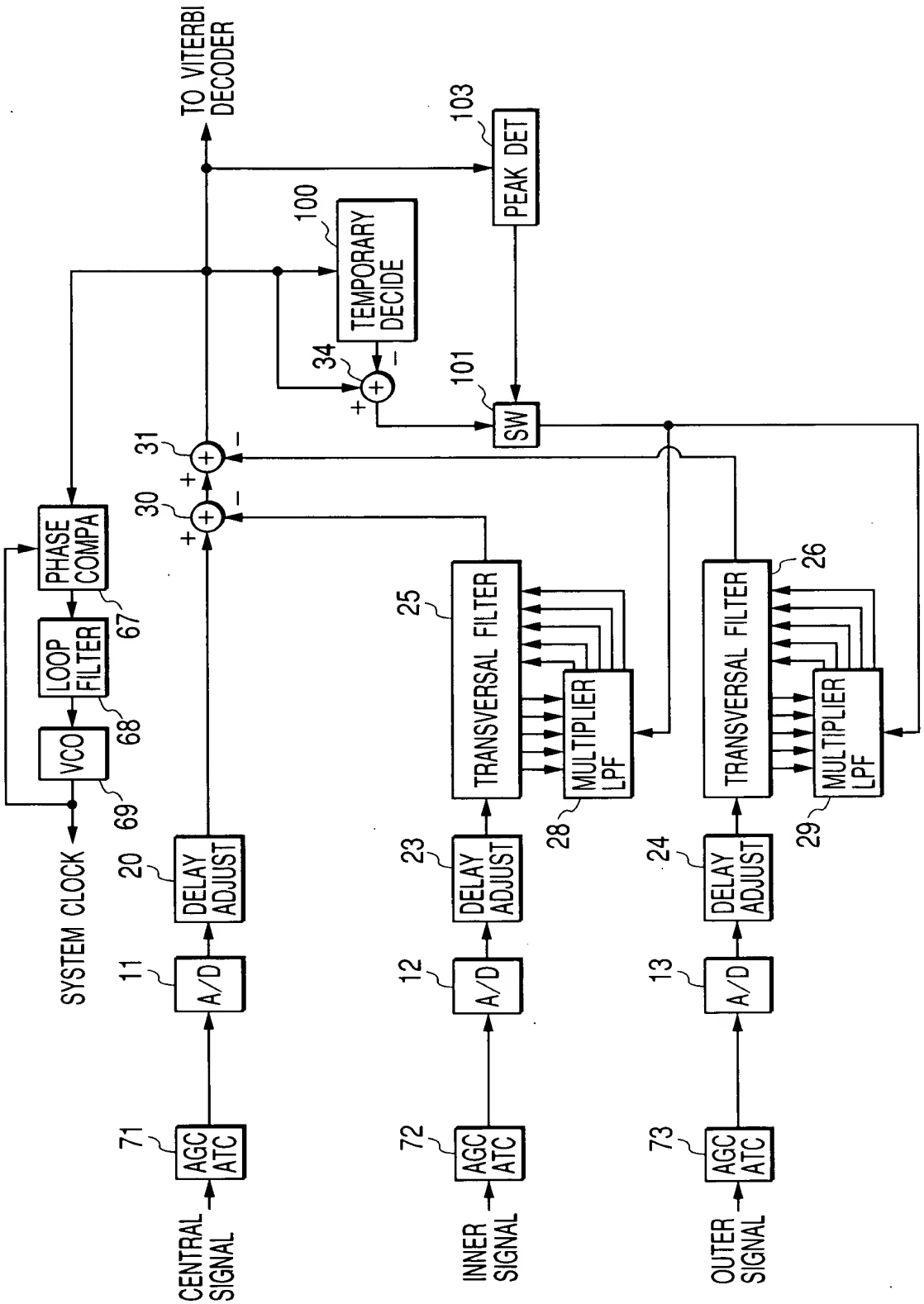

TO VITERBI DECODER
103
PEAK DET
100
TEMPORARY DECIDE
34
101
SW
31
30
PHASE COMPA
67
LOOP FILTER
68
VCO
69
SYSTEM CLOCK
20
DELAY ADJUST
11
A/D
71
AGC ATC
CENTRAL SIGNAL
25
TRANSVERSAL FILTER
MULTIPLIER LPF
28
23
DELAY ADJUST
12
A/D
72
AGC ATC
INNER SIGNAL
26
TRANSVERSAL FILTER
MULTIPLIER LPF
29
24
DELAY ADJUST
13
A/D
73
AGC ATC
OUTER SIGNAL

FIG. 32

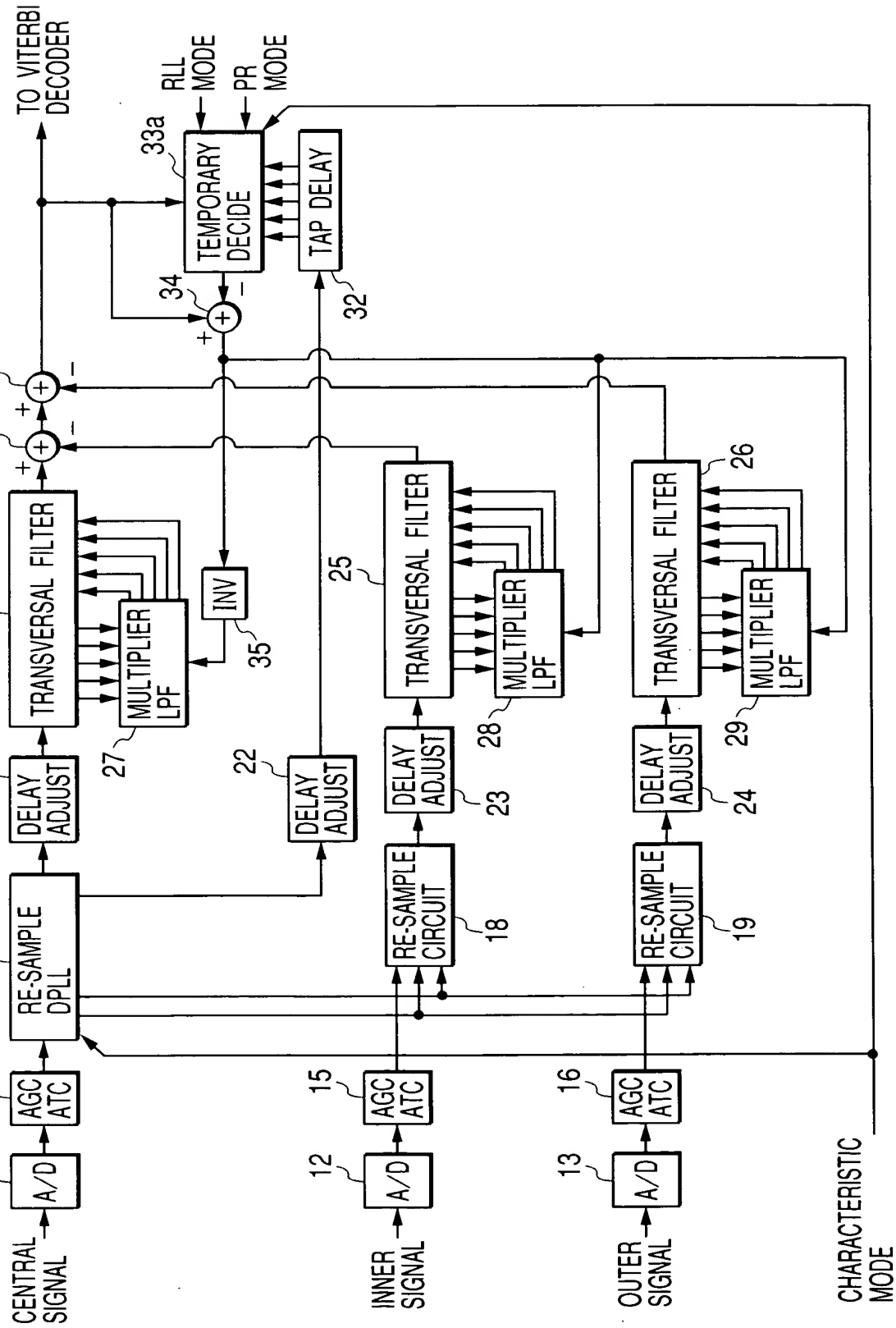

TO VITERBI DECODER
RLL MODE
PR MODE
33a
TEMPORARY DECIDE
TAP DELAY
34
32
31
30
TRANSVERSAL FILTER
21
MULTIPLIER LPF
27
INV
35
DELAY ADJUST
20
22
RE-SAMPLE DPLL
17a
AGC ATC
14
A/D
11
CENTRAL SIGNAL
25
TRANSVERSAL FILTER
MULTIPLIER LPF
28
DELAY ADJUST
23
RE-SAMPLE CIRCUIT
18
AGC ATC
15
A/D
12
INNER SIGNAL
26
TRANSVERSAL FILTER
MULTIPLIER LPF
29
DELAY ADJUST
24
RE-SAMPLE CIRCUIT
19
AGC ATC
16
A/D
13
OUTER SIGNAL
CHARACTERISTIC MODE

FIG. 33

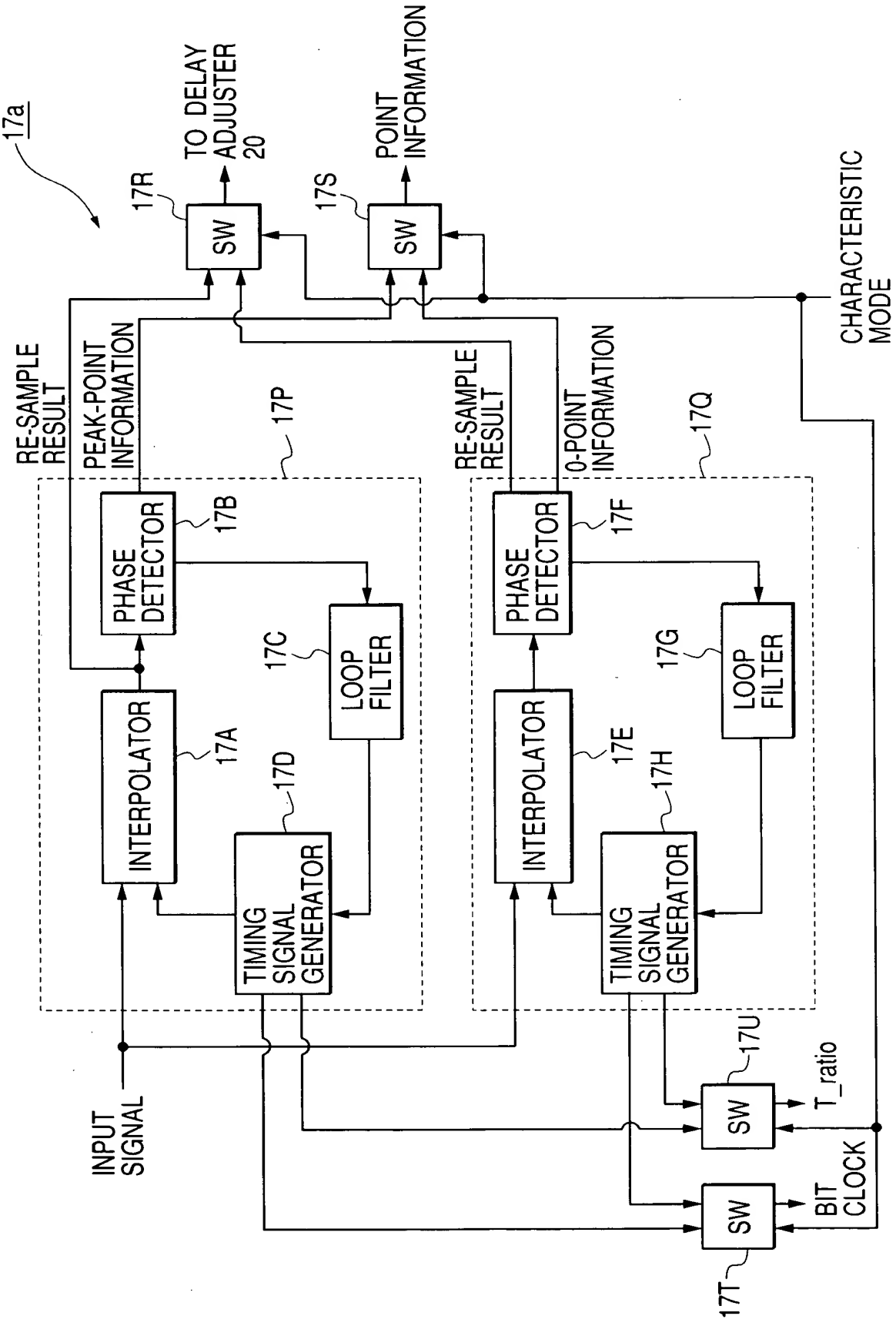

17a
TO DELAY ADJUSTER 20
POINT INFORMATION
17R
17S
SW
SW
CHARACTERISTIC MODE
RE-SAMPLE RESULT
PEAK-POINT INFORMATION
RE-SAMPLE RESULT
0-POINT INFORMATION
17P
17Q
PHASE DETECTOR
17B
PHASE DETECTOR
17F
LOOP FILTER
17C
LOOP FILTER
17G
INTERPOLATOR
17A
INTERPOLATOR
17E
TIMING SIGNAL GENERATOR
17D
TIMING SIGNAL GENERATOR
17H
INPUT SIGNAL
SW
17U
T_ratio
SW
BIT CLOCK
17T

FIG. 34

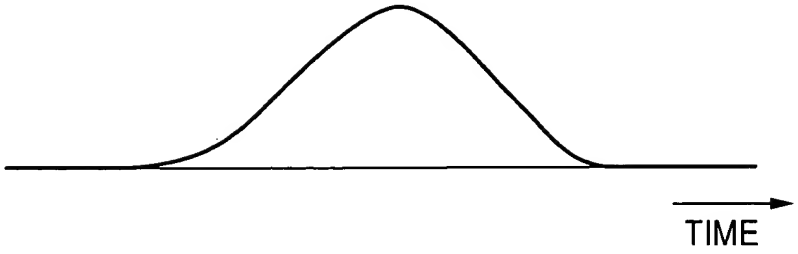


FIG. 35

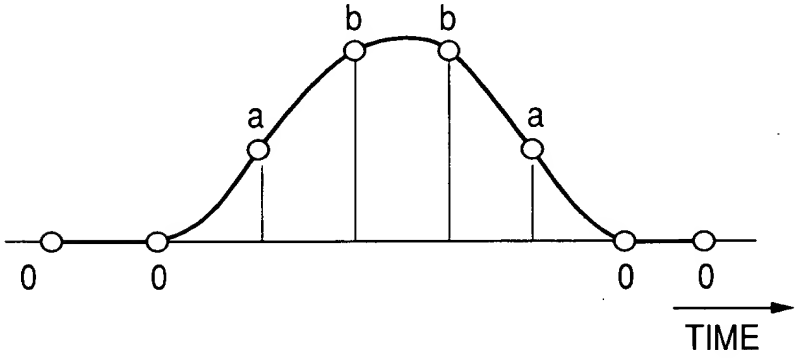


FIG. 36

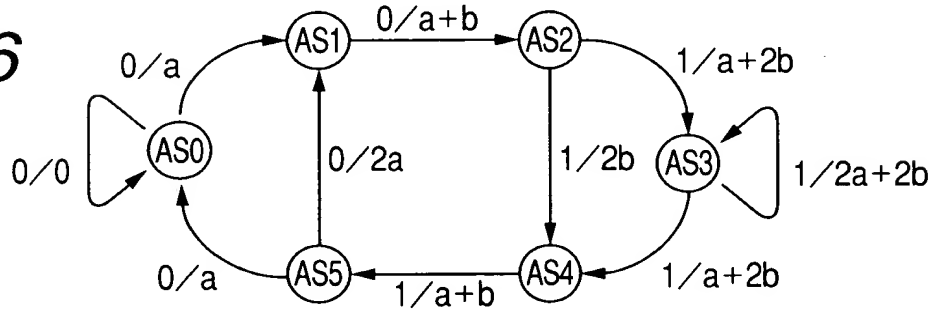


FIG. 37

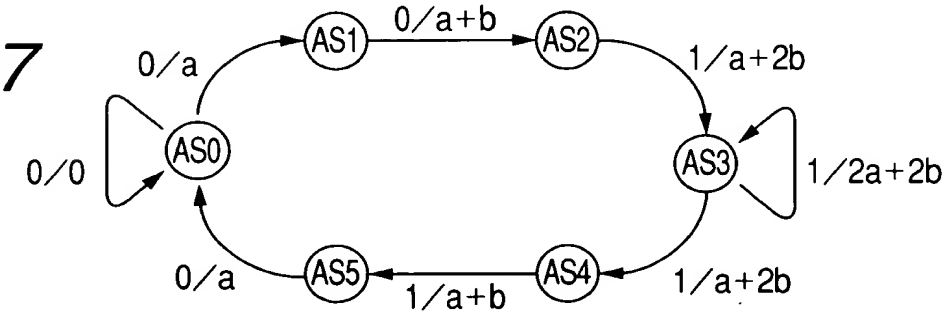


FIG. 38

RLL MODE \ PR MODE		1	2	3	4	5	6
RLL(1, X) {M1—7, MMVF, MD2}		PR(1, 1)	PR(1, 1, 1, 1)	PR(1, 2, 2, 1)	PR(1, 3, 3, 1)	PR(2, 3, 3, 2)	PR(3, 4, 4, 3)
	2a+2b			6→+3	8→+4	10→+5	14→+7
	a+2b			5→+2	7→+3	8→+3	11→+4
	2b			4→+1	6→+2	6→+1	8→+1
	a+b			3→ 0	4→ 0	5→ 0	7→ 0
	2a			2→−1	2→−2	4→−1	6→−1
	a			1→−2	1→−3	2→−3	3→−4
	0			0→−3	0→−4	0→−5	0→−7
	GAIN G	A	A/2	A/3	A/4	A/5	A/7
RLL(2, X) {EFM, EFMP, M8—15, PR}	2a+2b		4→+2	6→+3	8→+4	10→+5	14→+7
	a+2b	2→+1	3→+1	5→+2	7→+3	8→+3	11→+4
	a+b	1→ 0	2→ 0	3→ 0	4→ 0	5→ 0	7→ 0
	a	0→−1	1→−1	1→−2	1→−3	2→−3	3→−4
	0		0→−2	0→−3	0→−4	0→−5	0→−7

FIG. 39

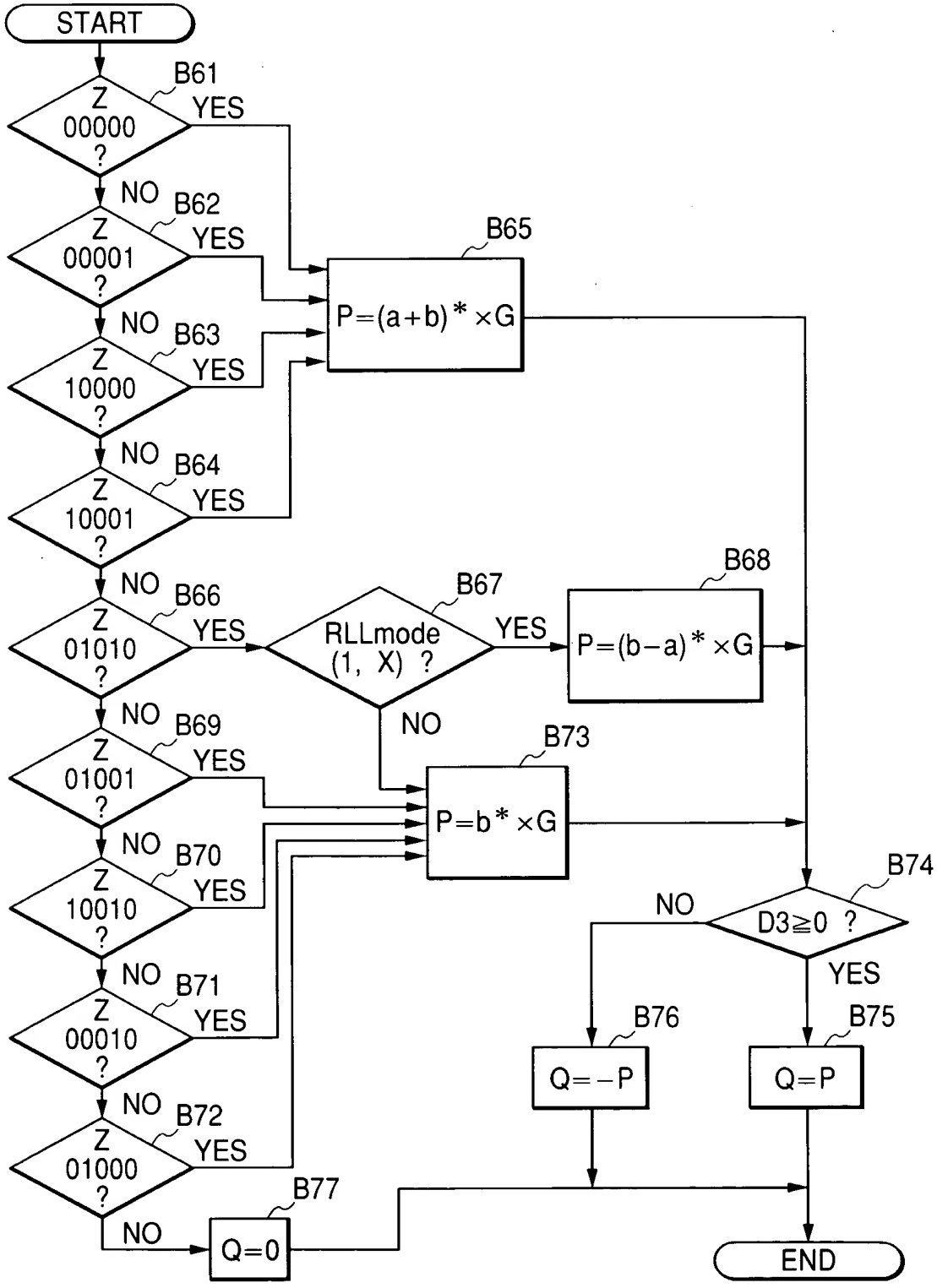

START
B61
Z 00000 ?
YES
NO
B62
Z 00001 ?
YES
NO
B63
Z 10000 ?
YES
NO
B64
Z 10001 ?
YES
NO
B65
P=(a+b)* ×G
B66
Z 01010 ?
YES
NO
B67
RLLmode (1, X) ?
YES
NO
B68
P=(b−a)* ×G
B69
Z 01001 ?
YES
NO
B70
Z 10010 ?
YES
NO
B71
Z 00010 ?
YES
NO
B72
Z 01000 ?
YES
NO
B73
P=b* ×G
B74
D3≧0 ?
YES
NO
B75
Q=P
B76
Q=−P
B77
Q=0
END

FIG. 40

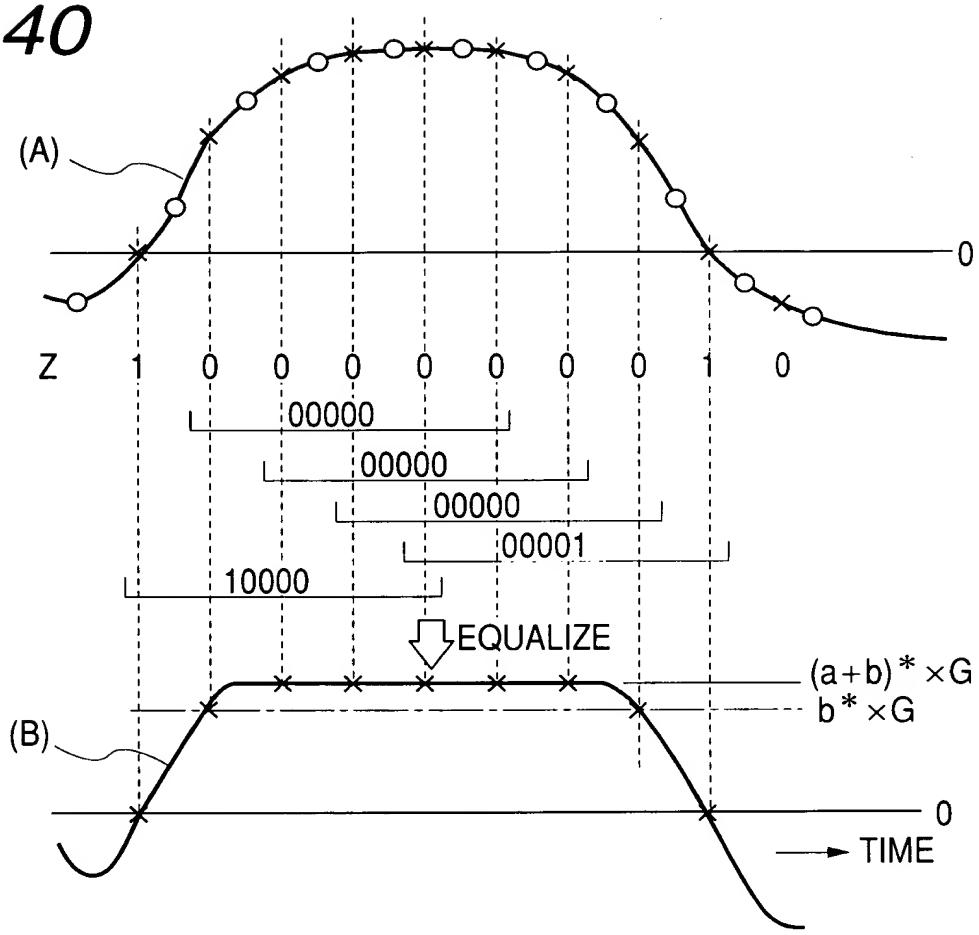

(A)
0
Z 1 0 0 0 0 0 0 0 1 0
00000
00000
00000
00001
10000
EQUALIZE
(a+b)*×G
b*×G
(B)
0
TIME

FIG. 41

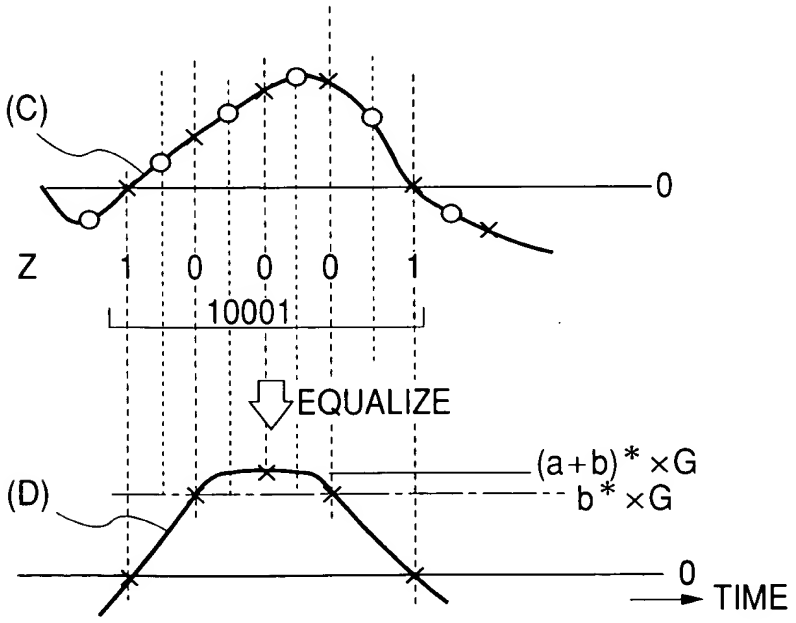

(C)
0
Z 1 0 0 0 1
10001
EQUALIZE
(a+b)*×G
b*×G
(D)
0
TIME

FIG. 42

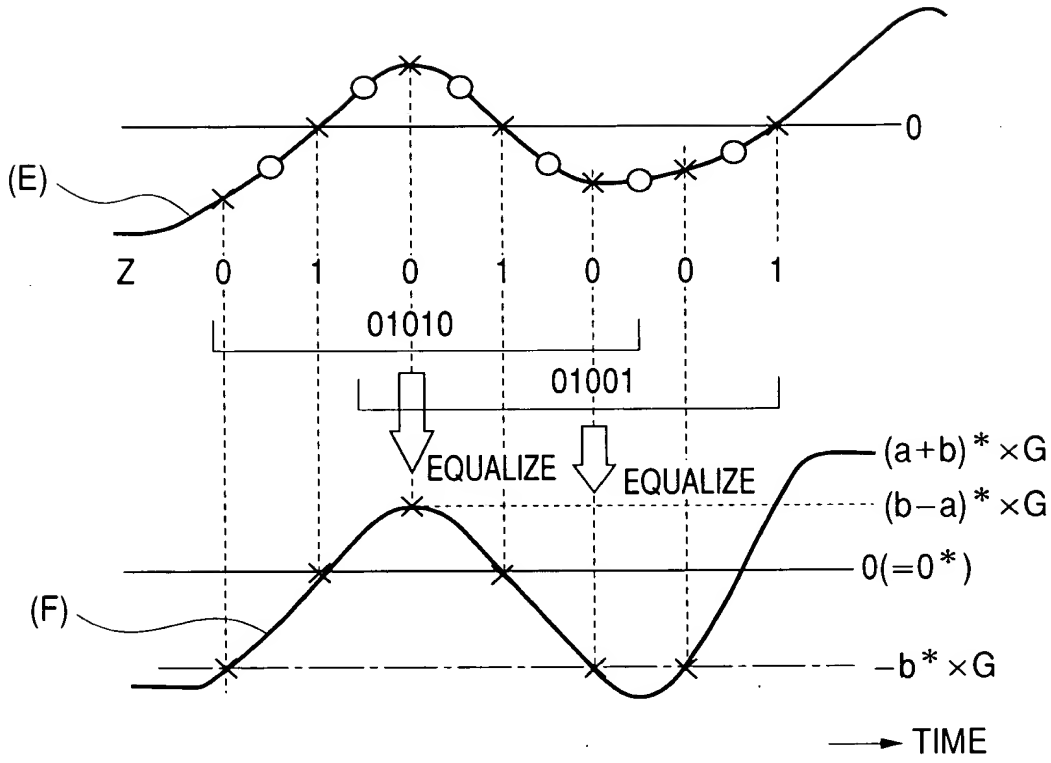

(E)
0
Z
0
1
0
1
0
0
1
01010
01001
EQUALIZE
EQUALIZE
(a+b)*×G
(b−a)*×G
0(=0*)
(F)
−b*×G
TIME

FIG. 43

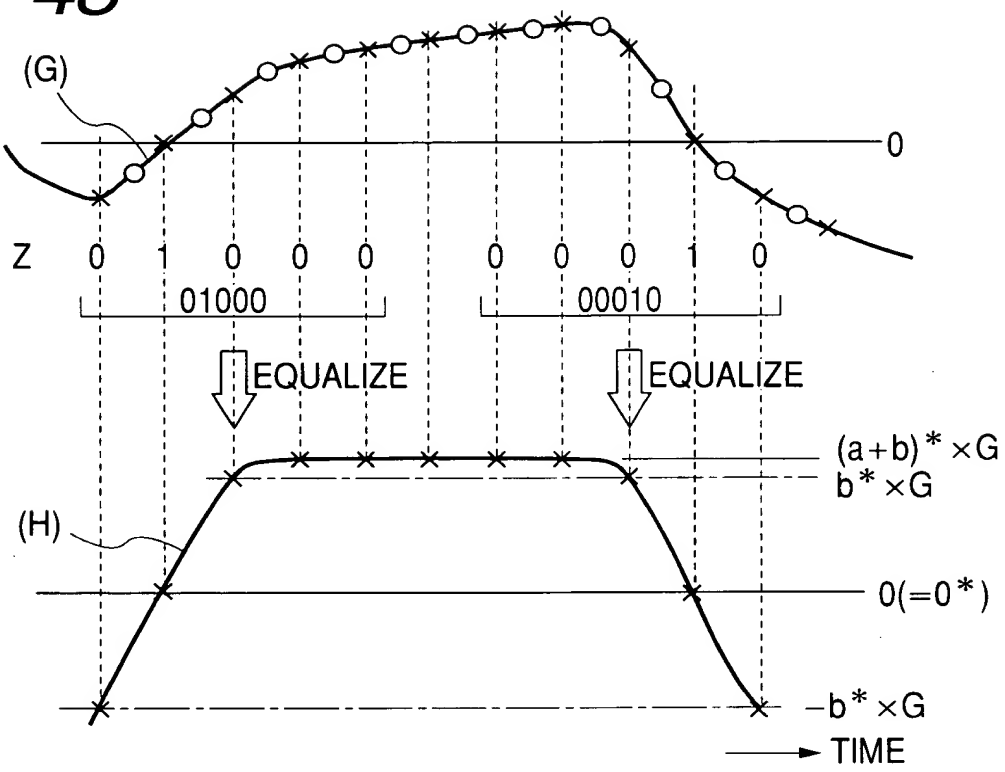

(G)
0
Z 0 1 0 0 0 0 0 0 1 0
01000
00010
EQUALIZE
EQUALIZE
(a+b)* ×G
b* ×G
(H)
0(=0*)
−b* ×G
TIME

FIG. 44

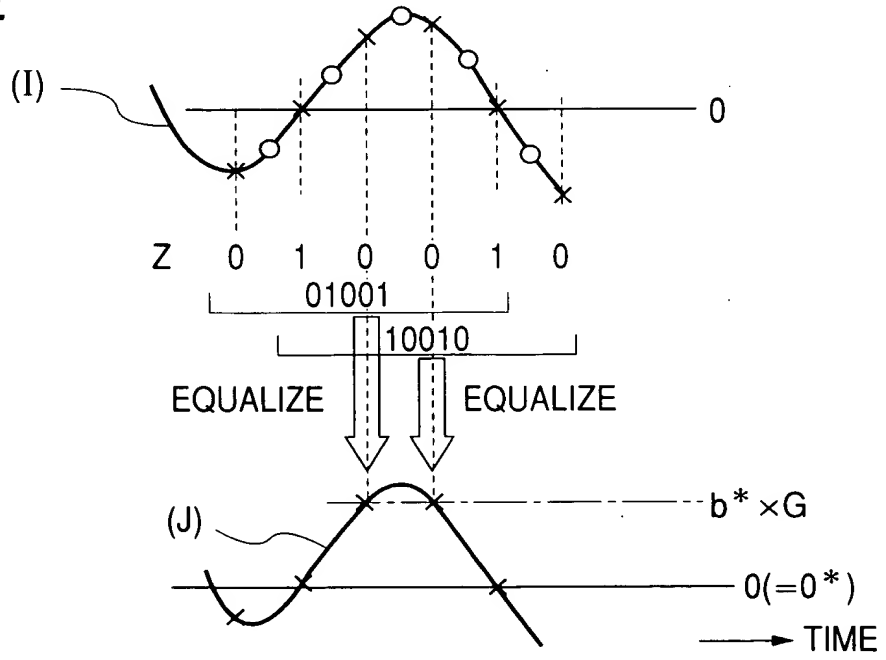

(I)
0
Z 0 1 0 0 1 0
01001
10010
EQUALIZE
EQUALIZE
b* ×G
(J)
0(=0*)
TIME

FIG. 45

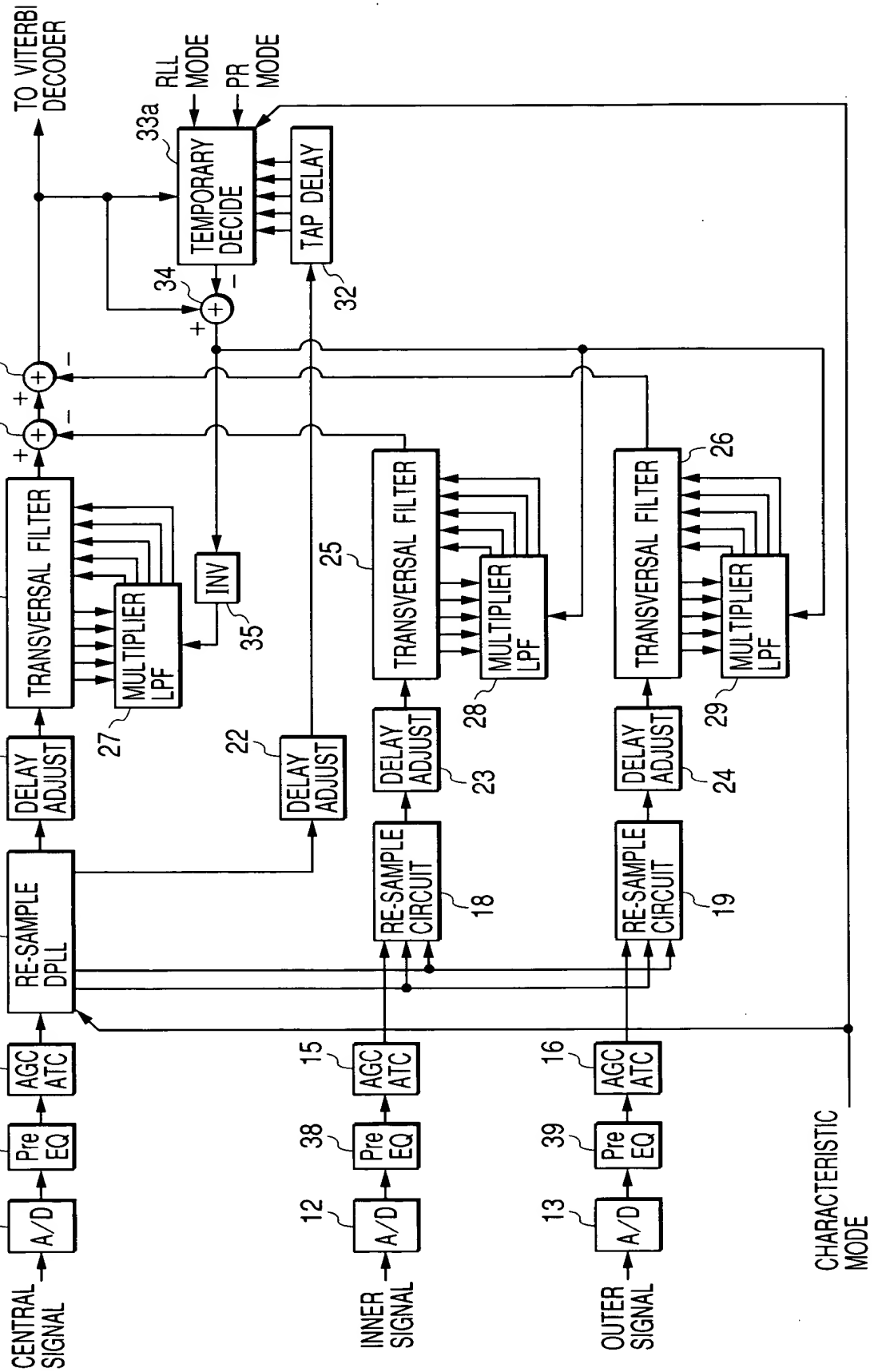

TO VITERBI DECODER
RLL MODE
PR MODE
33a
TEMPORARY DECIDE
TAP DELAY
34
32
31
30
TRANSVERSAL FILTER
MULTIPLIER LPF
INV
35
21
27
20
DELAY ADJUST
22
DELAY ADJUST
25
TRANSVERSAL FILTER
MULTIPLIER LPF
28
DELAY ADJUST
23
26
TRANSVERSAL FILTER
MULTIPLIER LPF
29
DELAY ADJUST
24
17a
RE-SAMPLE DPLL
RE-SAMPLE CIRCUIT
18
RE-SAMPLE CIRCUIT
19
14
AGC ATC
15
AGC ATC
16
AGC ATC
37
Pre EQ
38
Pre EQ
39
Pre EQ
11
A/D
12
A/D
13
A/D
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL
CHARACTERISTIC MODE

FIG. 46

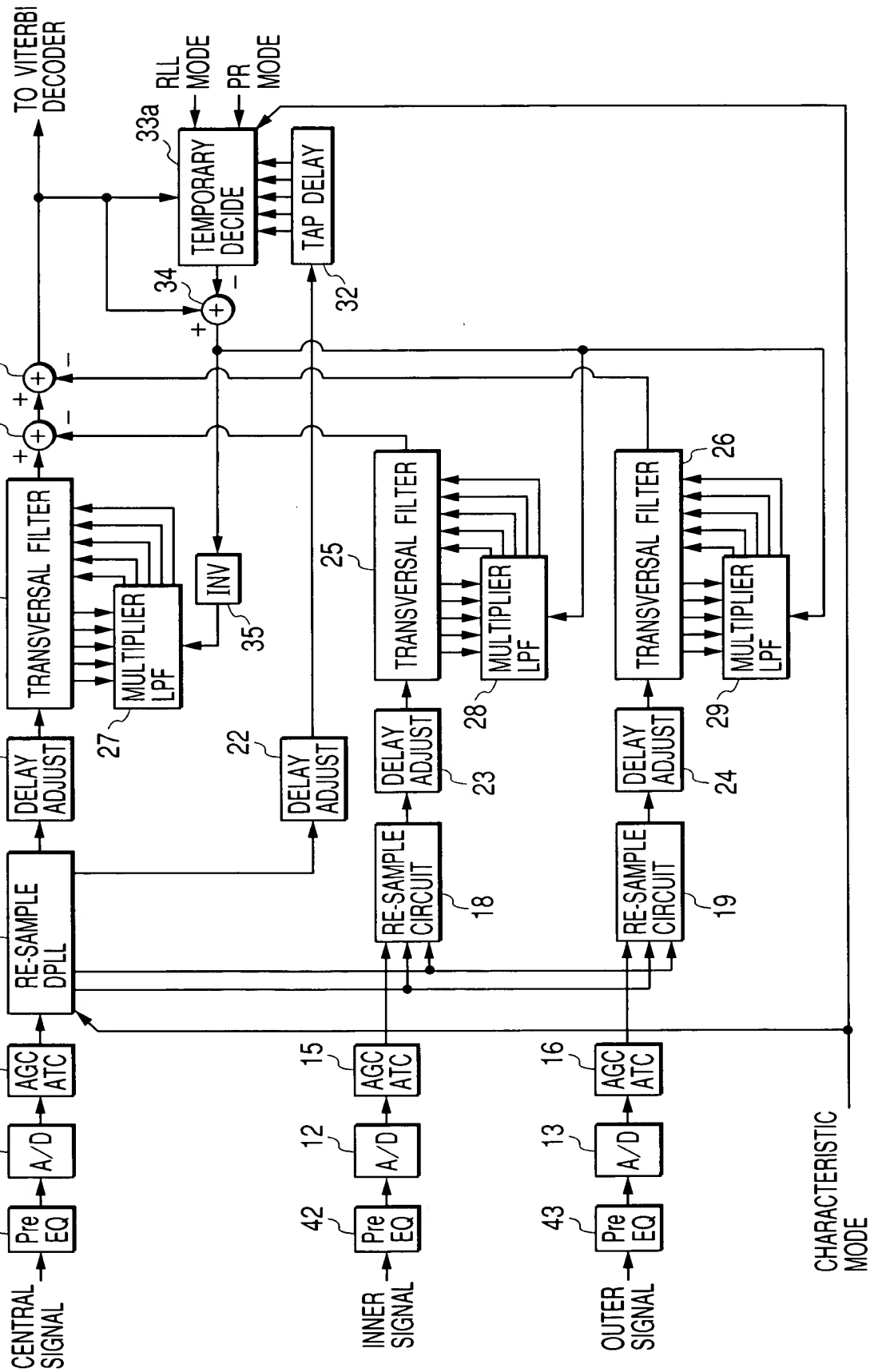

TO VITERBI DECODER
RLL MODE
PR MODE
33a
TEMPORARY DECIDE
TAP DELAY
34
32
31
30
TRANSVERSAL FILTER
21
MULTIPLIER LPF
27
INV
35
DELAY ADJUST
20
22
RE-SAMPLE DPLL
17a
25
TRANSVERSAL FILTER
MULTIPLIER LPF
28
DELAY ADJUST
23
RE-SAMPLE CIRCUIT
18
26
TRANSVERSAL FILTER
MULTIPLIER LPF
29
DELAY ADJUST
24
RE-SAMPLE CIRCUIT
19
AGC ATC
14
15
16
A/D
11
12
13
Pre EQ
41
42
43
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL
CHARACTERISTIC MODE

FIG. 47

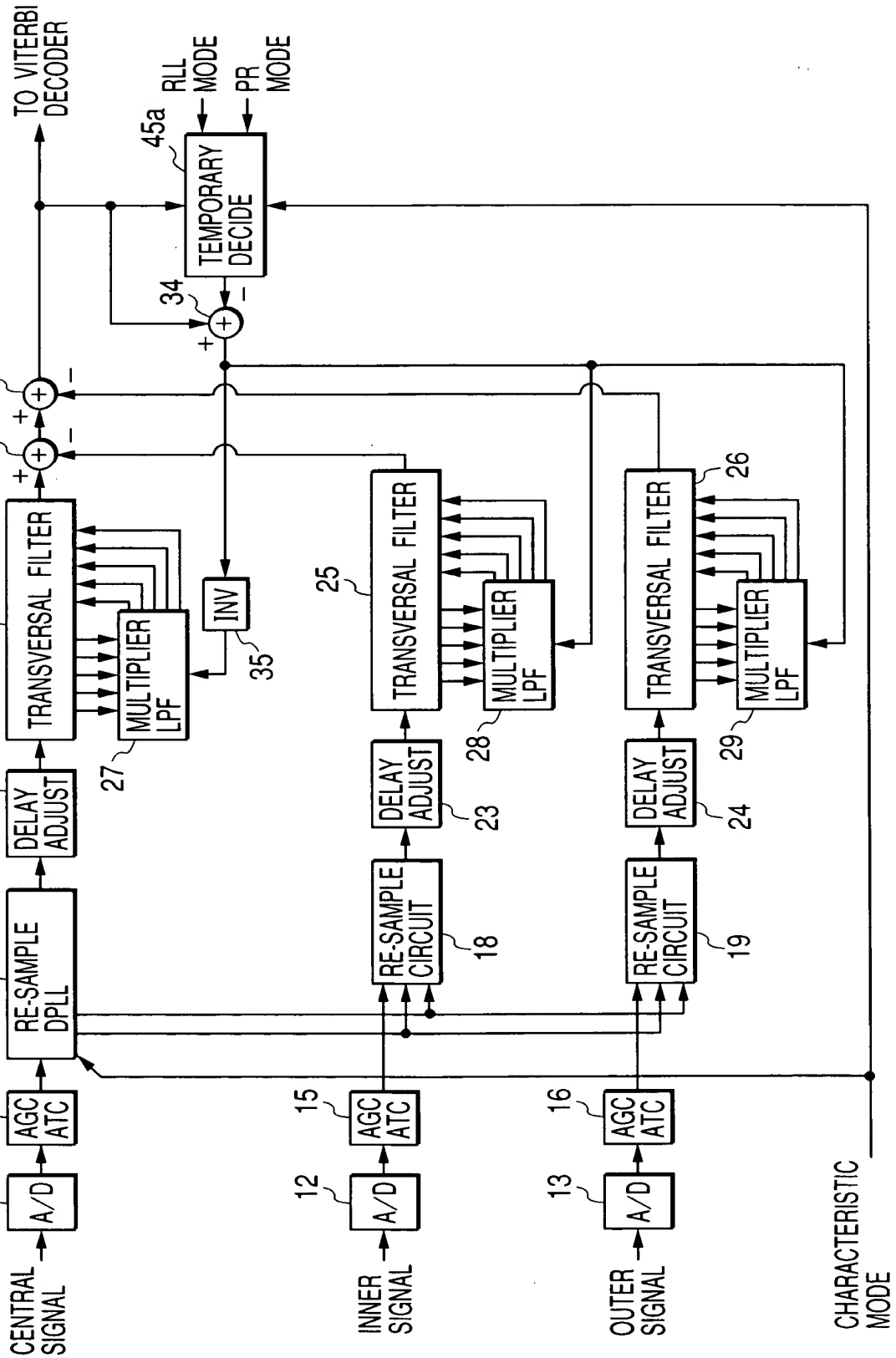

TO VITERBI DECODER
RLL MODE
PR MODE
45a
TEMPORARY DECIDE
34
31
30
TRANSVERSAL FILTER
21
MULTIPLIER LPF
27
INV
35
DELAY ADJUST
20
RE-SAMPLE DPLL
17a
AGC ATC
14
A/D
11
CENTRAL SIGNAL
TRANSVERSAL FILTER
25
MULTIPLIER LPF
28
DELAY ADJUST
23
RE-SAMPLE CIRCUIT
18
AGC ATC
15
A/D
12
INNER SIGNAL
TRANSVERSAL FILTER
26
MULTIPLIER LPF
29
DELAY ADJUST
24
RE-SAMPLE CIRCUIT
19
AGC ATC
16
A/D
13
OUTER SIGNAL
CHARACTERISTIC MODE

FIG. 48

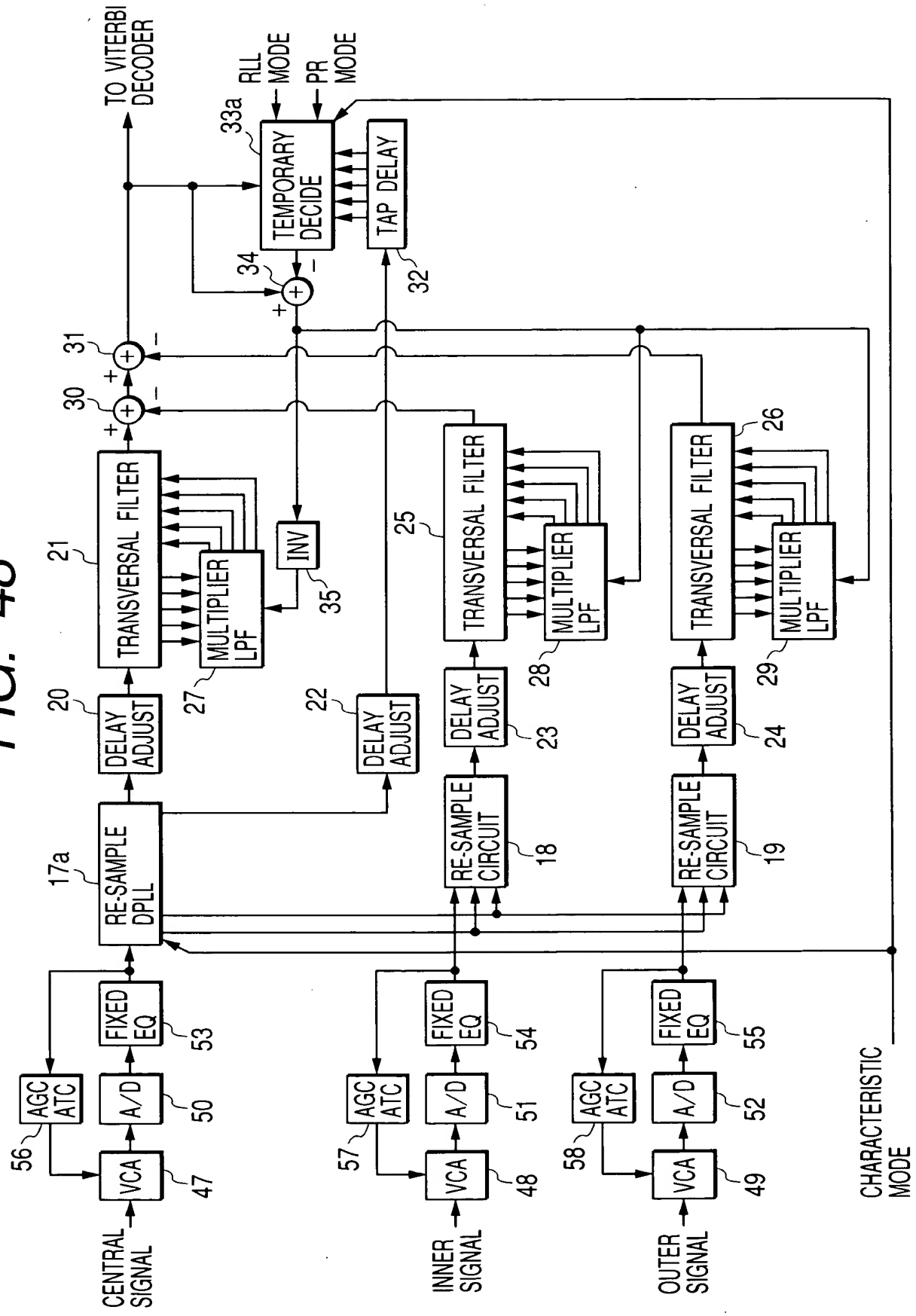

TO VITERBI DECODER
33a
RLL MODE
PR MODE
TEMPORARY DECIDE
TAP DELAY
34
32
31
30
21
TRANSVERSAL FILTER
MULTIPLIER LPF
27
INV
35
25
TRANSVERSAL FILTER
MULTIPLIER LPF
28
26
TRANSVERSAL FILTER
MULTIPLIER LPF
29
20
DELAY ADJUST
22
DELAY ADJUST
23
DELAY ADJUST
24
17a
RE-SAMPLE DPLL
RE-SAMPLE CIRCUIT
18
RE-SAMPLE CIRCUIT
19
FIXED EQ
53
FIXED EQ
54
FIXED EQ
55
AGC ATC
56
A/D
50
AGC ATC
57
A/D
51
AGC ATC
58
A/D
52
VCA
47
VCA
48
VCA
49
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL
CHARACTERISTIC MODE

FIG. 49

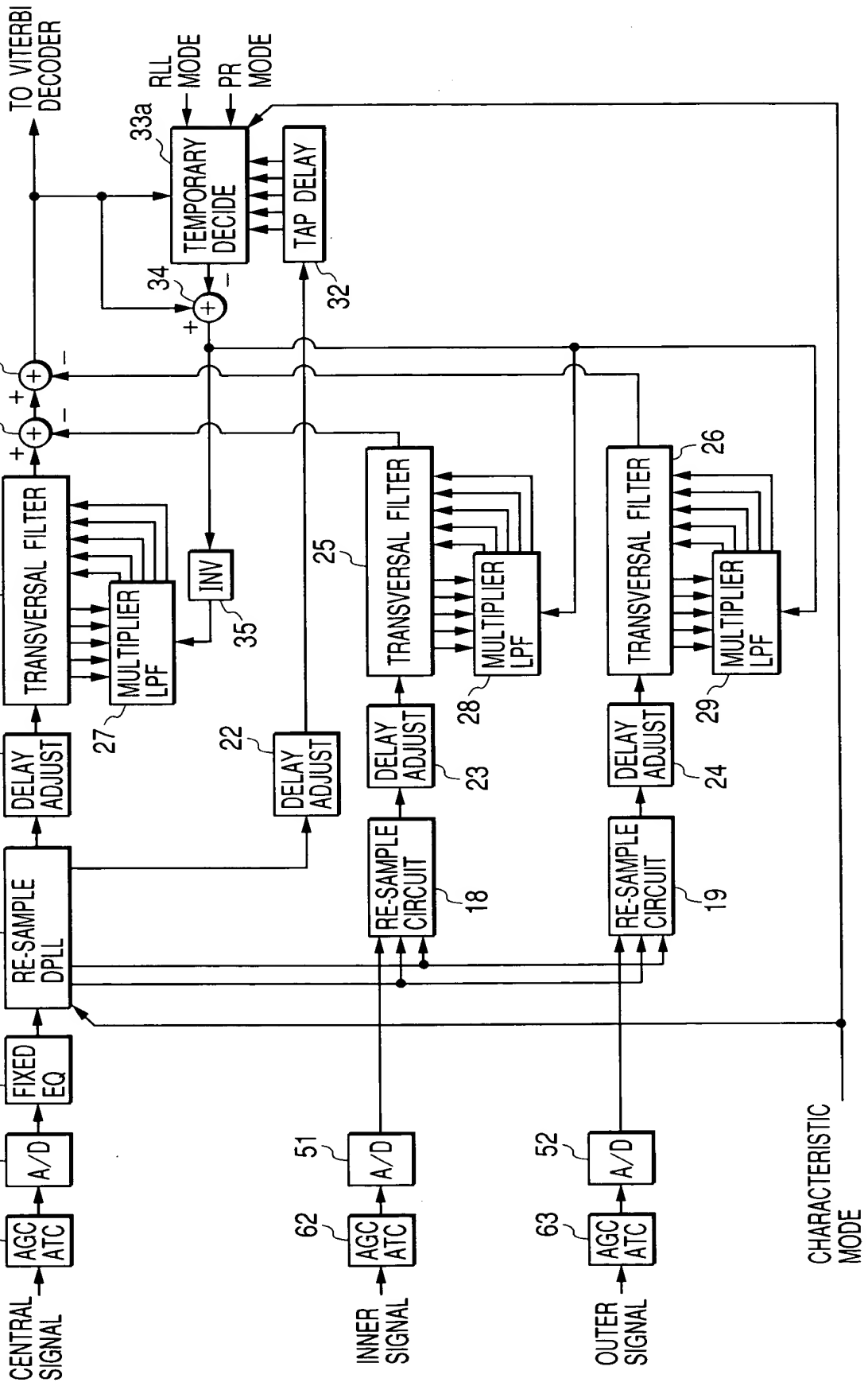

TO VITERBI DECODER
RLL MODE
PR MODE
33a
TEMPORARY DECIDE
TAP DELAY
34
32
31
30
21
TRANSVERSAL FILTER
MULTIPLIER LPF
27
INV
35
25
TRANSVERSAL FILTER
MULTIPLIER LPF
28
26
TRANSVERSAL FILTER
MULTIPLIER LPF
29
20
DELAY ADJUST
22
DELAY ADJUST
23
DELAY ADJUST
24
17a
RE-SAMPLE DPLL
RE-SAMPLE CIRCUIT
18
RE-SAMPLE CIRCUIT
19
53
FIXED EQ
50
A/D
51
A/D
52
A/D
61
AGC ATC
62
AGC ATC
63
AGC ATC
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL
CHARACTERISTIC MODE

FIG. 50

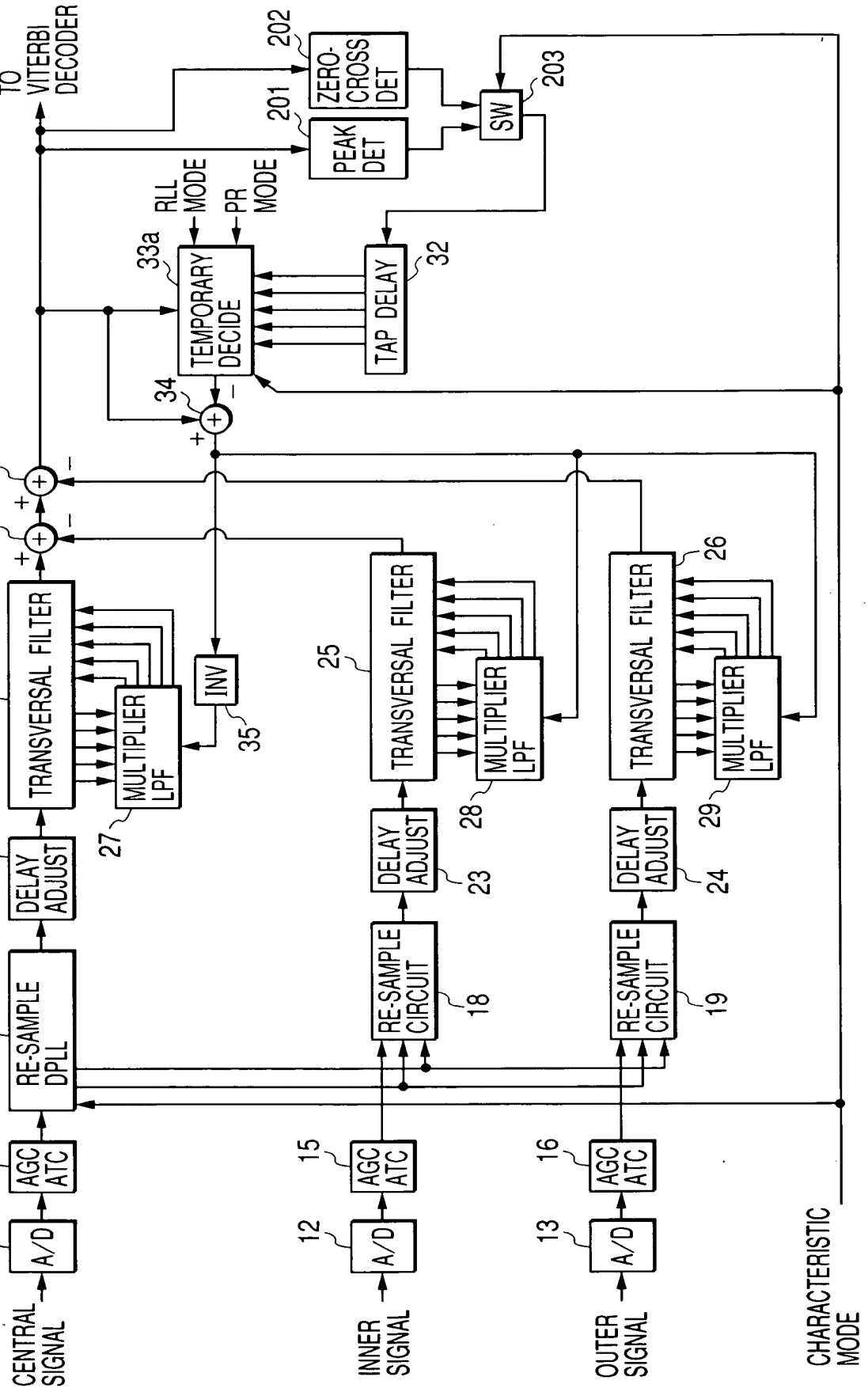

TO VITERBI DECODER
202
ZERO-CROSS DET
201
PEAK DET
203
SW
RLL MODE
PR MODE
33a
TEMPORARY DECIDE
32
TAP DELAY
34
31
30
21
TRANSVERSAL FILTER
MULTIPLIER LPF
27
INV
35
20
DELAY ADJUST
17a
RE-SAMPLE DPLL
14
AGC ATC
11
A/D
CENTRAL SIGNAL
25
TRANSVERSAL FILTER
MULTIPLIER LPF
28
DELAY ADJUST
23
RE-SAMPLE CIRCUIT
18
15
AGC ATC
12
A/D
INNER SIGNAL
26
TRANSVERSAL FILTER
MULTIPLIER LPF
29
DELAY ADJUST
24
RE-SAMPLE CIRCUIT
19
16
AGC ATC
13
A/D
OUTER SIGNAL
CHARACTERISTIC MODE

FIG. 51

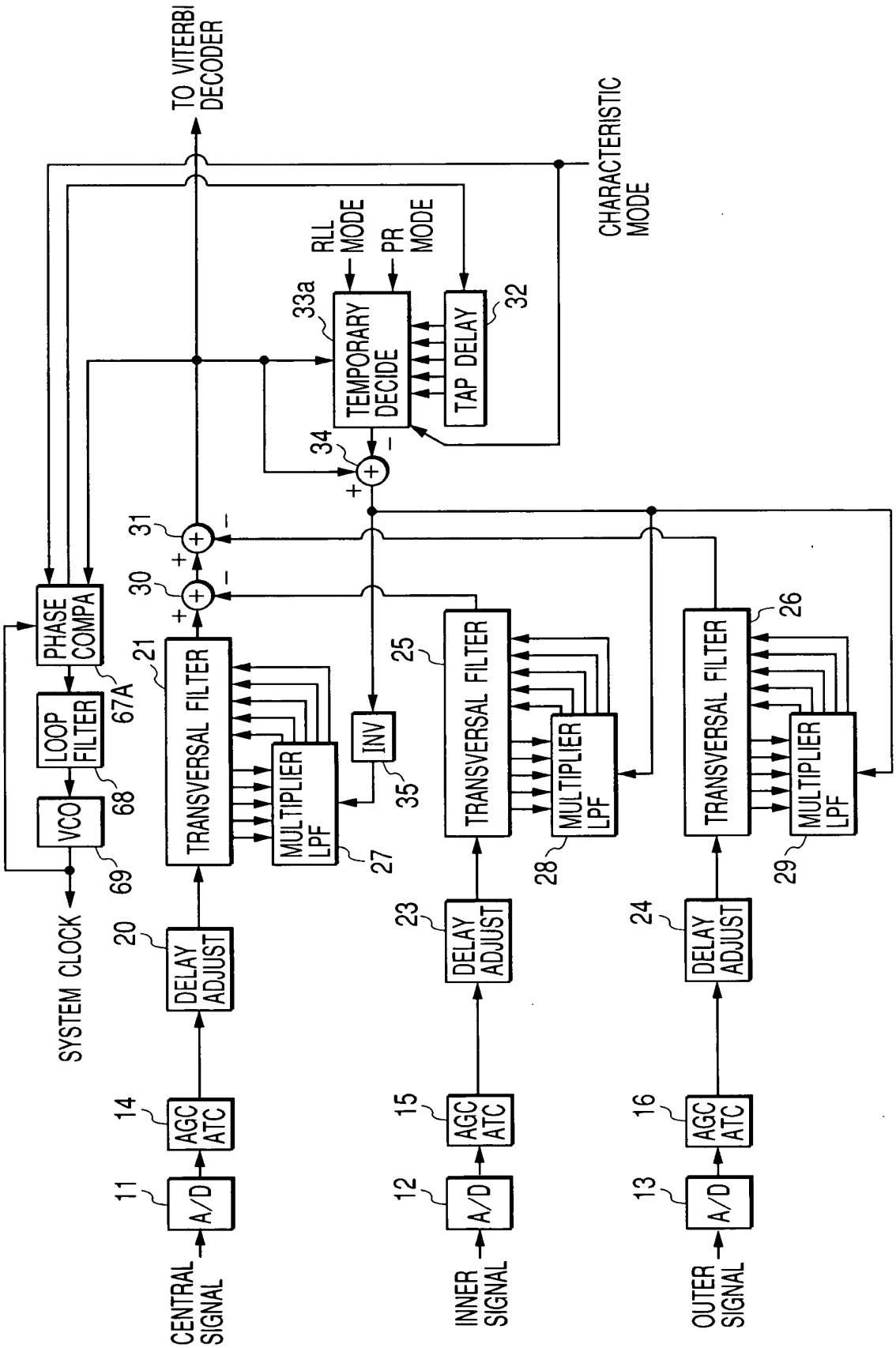

TO VITERBI DECODER
CHARACTERISTIC MODE
RLL MODE
PR MODE
33a
TEMPORARY DECIDE
TAP DELAY
32
34
31
30
PHASE COMPA
67A
LOOP FILTER
68
VCO
69
SYSTEM CLOCK
21
TRANSVERSAL FILTER
MULTIPLIER LPF
27
INV
35
25
TRANSVERSAL FILTER
MULTIPLIER LPF
28
26
TRANSVERSAL FILTER
MULTIPLIER LPF
29
20
DELAY ADJUST
23
DELAY ADJUST
24
DELAY ADJUST
14
AGC ATC
15
AGC ATC
16
AGC ATC
11
A/D
12
A/D
13
A/D
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL

FIG. 52

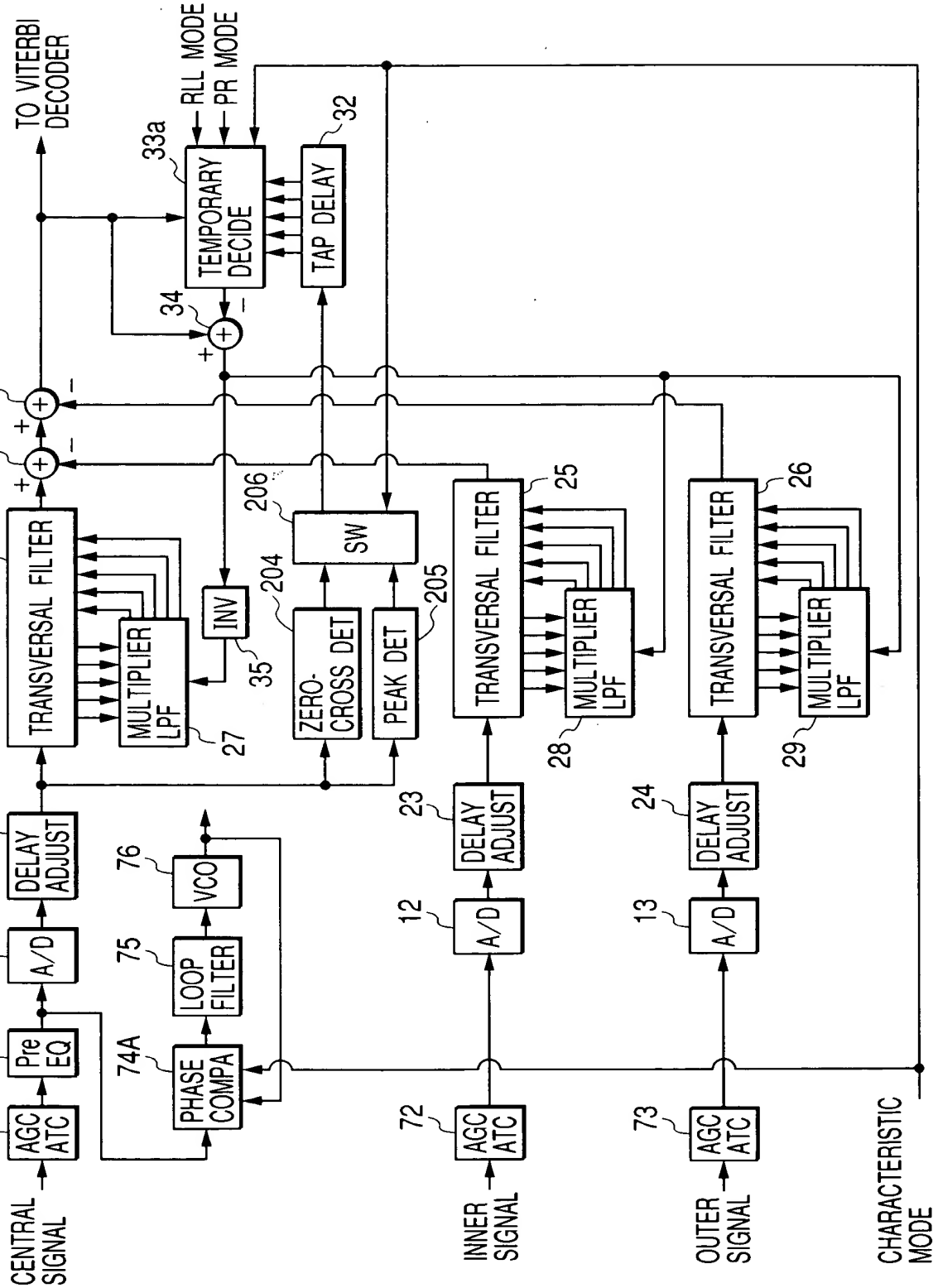

TO VITERBI DECODER
RLL MODE
PR MODE
33a
TEMPORARY DECIDE
TAP DELAY
32
34
31
30
21
TRANSVERSAL FILTER
MULTIPLIER LPF
27
INV
35
206
SW
204
ZERO-CROSS DET
205
PEAK DET
TRANSVERSAL FILTER
25
MULTIPLIER LPF
28
TRANSVERSAL FILTER
26
MULTIPLIER LPF
29
20
DELAY ADJUST
23
DELAY ADJUST
24
DELAY ADJUST
11
A/D
12
A/D
13
A/D
41
Pre EQ
74A
PHASE COMPA
75
LOOP FILTER
76
VCO
71
AGC ATC
72
AGC ATC
73
AGC ATC
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL
CHARACTERISTIC MODE

FIG. 53

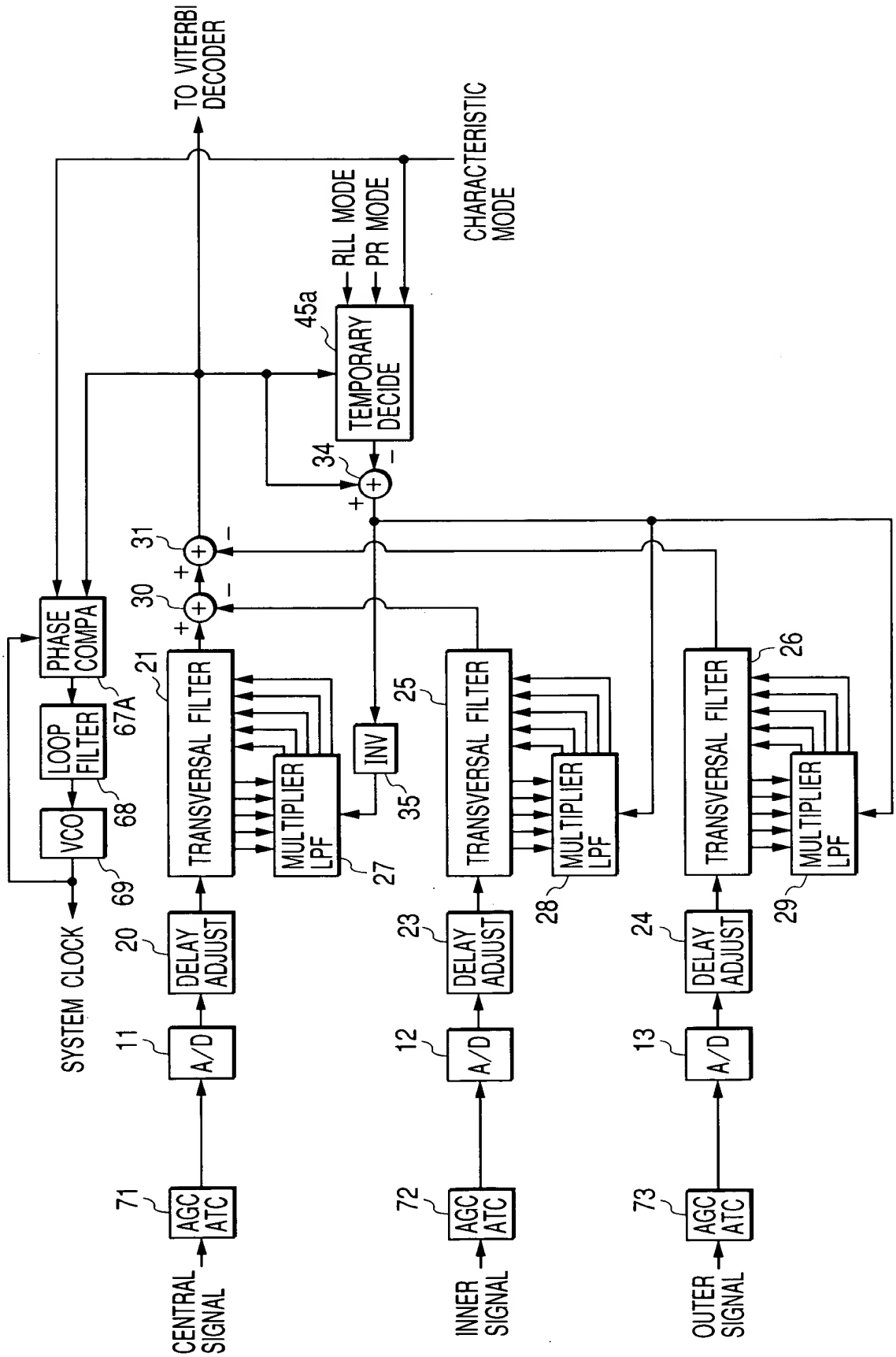

TO VITERBI DECODER
CHARACTERISTIC MODE
RLL MODE
PR MODE
45a
TEMPORARY DECIDE
34
31
30
PHASE COMPA
67A
LOOP FILTER
68
VCO
69
SYSTEM CLOCK
21
TRANSVERSAL FILTER
MULTIPLIER
LPF
27
INV
35
25
TRANSVERSAL FILTER
MULTIPLIER
LPF
28
26
TRANSVERSAL FILTER
MULTIPLIER
LPF
29
20
DELAY ADJUST
23
DELAY ADJUST
24
DELAY ADJUST
11
A/D
12
A/D
13
A/D
71
AGC ATC
72
AGC ATC
73
AGC ATC
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL

FIG. 54

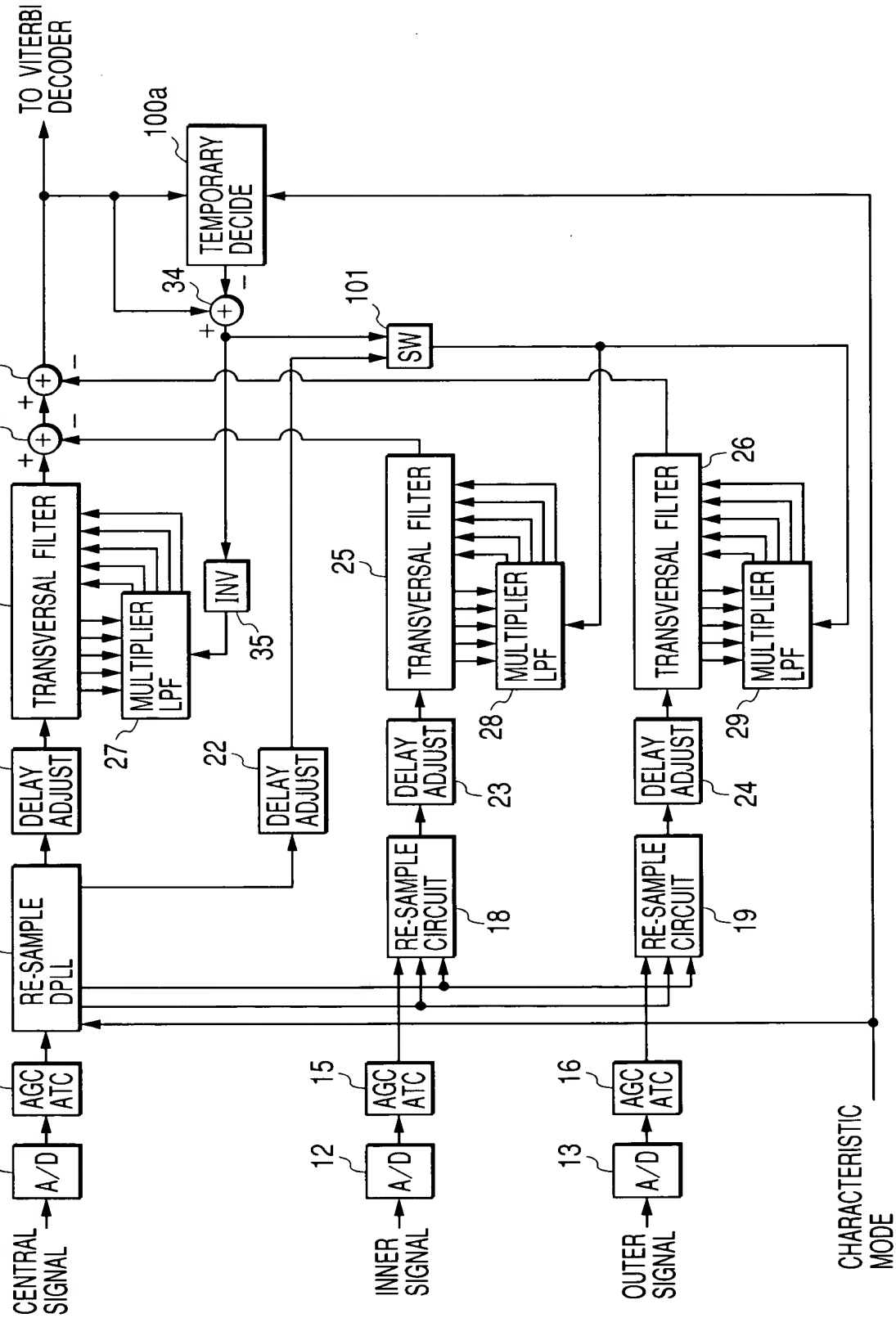

TO VITERBI DECODER
100a
TEMPORARY DECIDE
34
101
SW
31
30
21
TRANSVERSAL FILTER
MULTIPLIER LPF
27
INV
35
20
DELAY ADJUST
22
DELAY ADJUST
17a
RE-SAMPLE DPLL
14
AGC ATC
11
A/D
CENTRAL SIGNAL
25
TRANSVERSAL FILTER
MULTIPLIER LPF
28
23
DELAY ADJUST
RE-SAMPLE CIRCUIT
18
15
AGC ATC
12
A/D
INNER SIGNAL
26
TRANSVERSAL FILTER
MULTIPLIER LPF
29
24
DELAY ADJUST
RE-SAMPLE CIRCUIT
19
16
AGC ATC
13
A/D
OUTER SIGNAL
CHARACTERISTIC MODE

FIG. 55

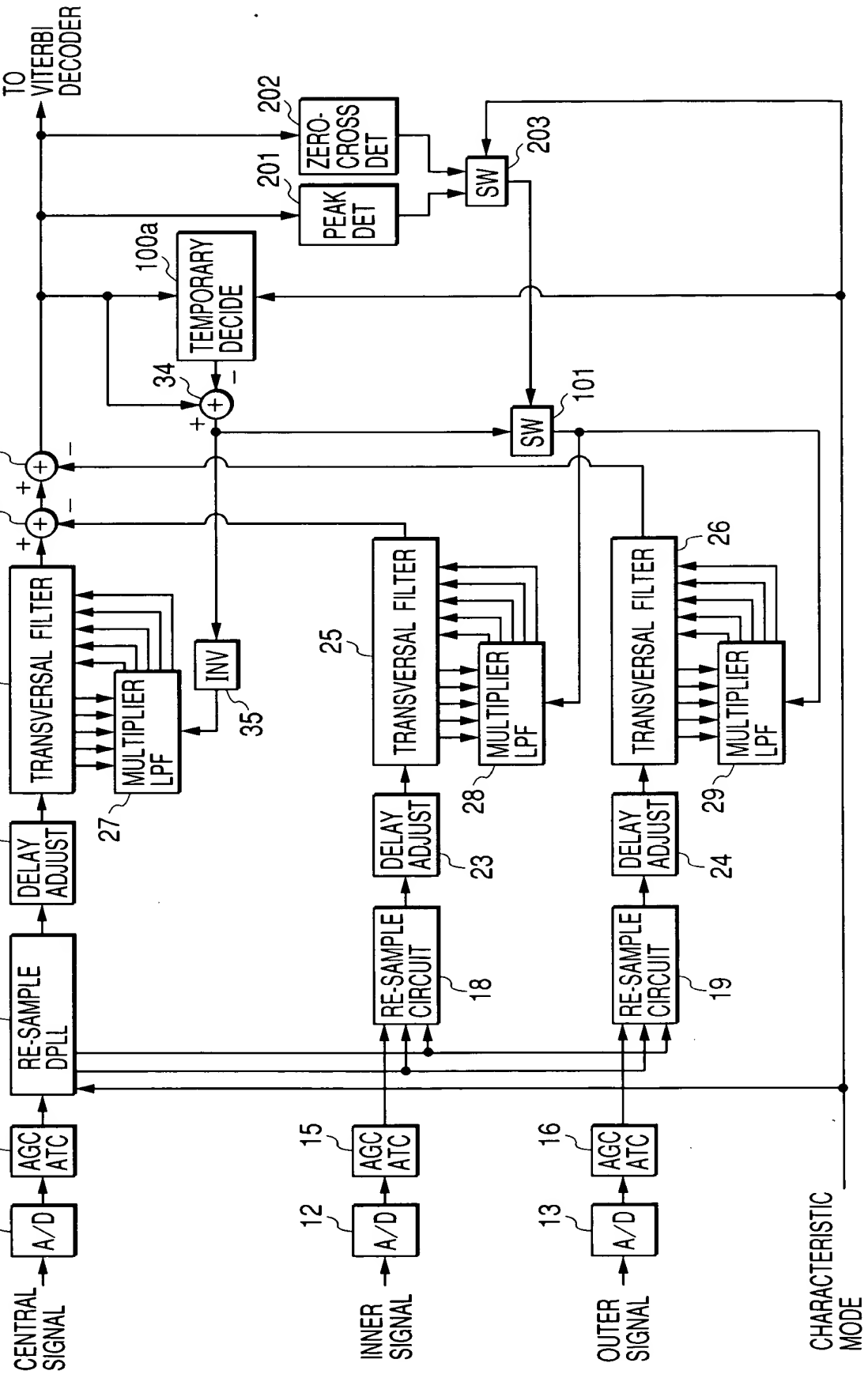

TO VITERBI DECODER
ZERO-CROSS DET
PEAK DET
SW
TEMPORARY DECIDE
SW
TRANSVERSAL FILTER
MULTIPLIER LPF
INV
TRANSVERSAL FILTER
MULTIPLIER LPF
TRANSVERSAL FILTER
MULTIPLIER LPF
DELAY ADJUST
DELAY ADJUST
DELAY ADJUST
RE-SAMPLE DPLL
RE-SAMPLE CIRCUIT
RE-SAMPLE CIRCUIT
AGC ATC
AGC ATC
AGC ATC
A/D
A/D
A/D
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL
CHARACTERISTIC MODE

FIG. 56

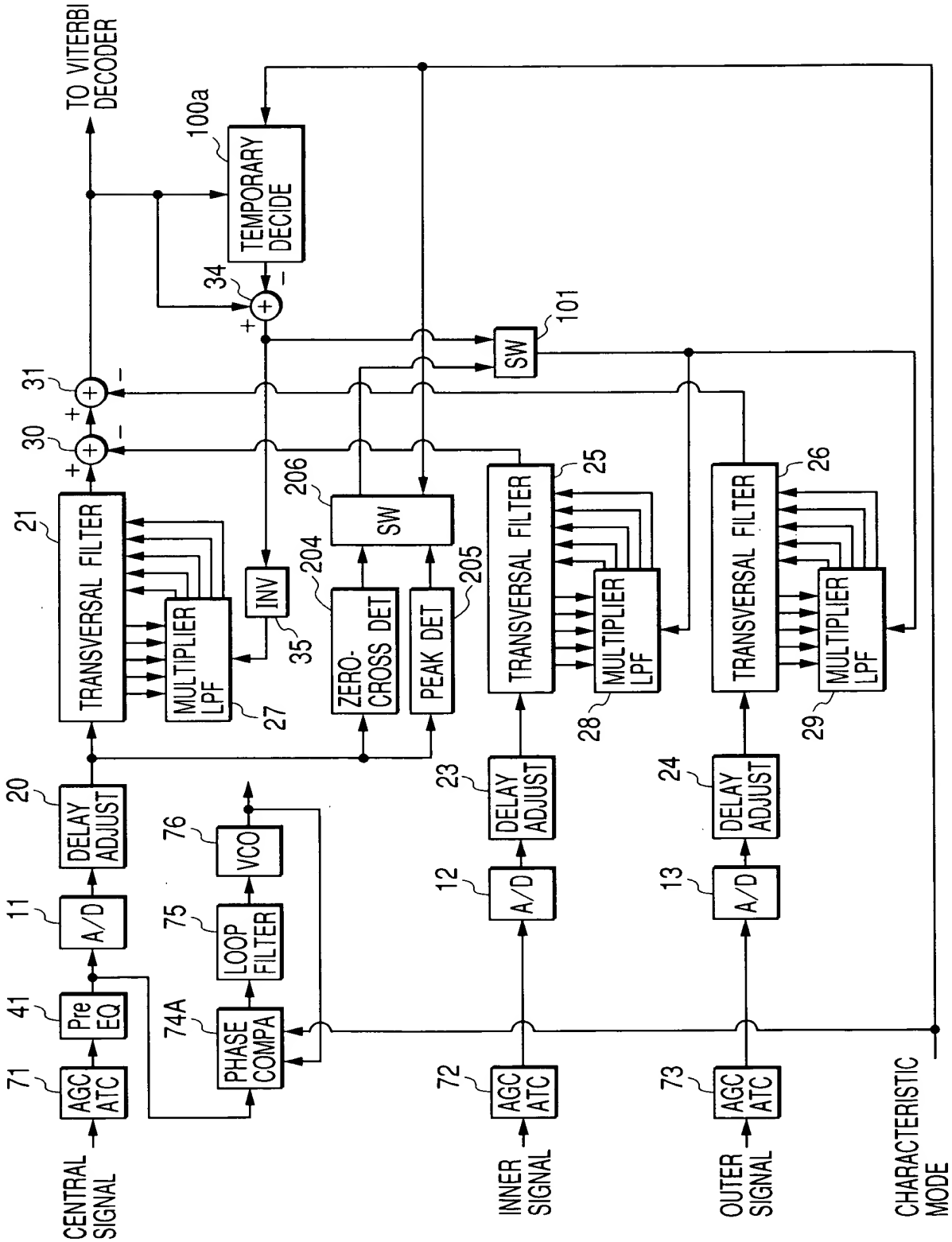

TO VITERBI DECODER
100a
TEMPORARY DECIDE
34
SW
101
31
30
21
TRANSVERSAL FILTER
MULTIPLIER LPF
27
INV
35
206
SW
204
ZERO-CROSS DET
205
PEAK DET
TRANSVERSAL FILTER
25
MULTIPLIER LPF
28
TRANSVERSAL FILTER
26
MULTIPLIER LPF
29
20
DELAY ADJUST
11
A/D
41
Pre EQ
71
AGC ATC
CENTRAL SIGNAL
76
VCO
75
LOOP FILTER
74A
PHASE COMPA
23
DELAY ADJUST
12
A/D
72
AGC ATC
INNER SIGNAL
24
DELAY ADJUST
13
A/D
73
AGC ATC
OUTER SIGNAL
CHARACTERISTIC MODE

FIG. 57

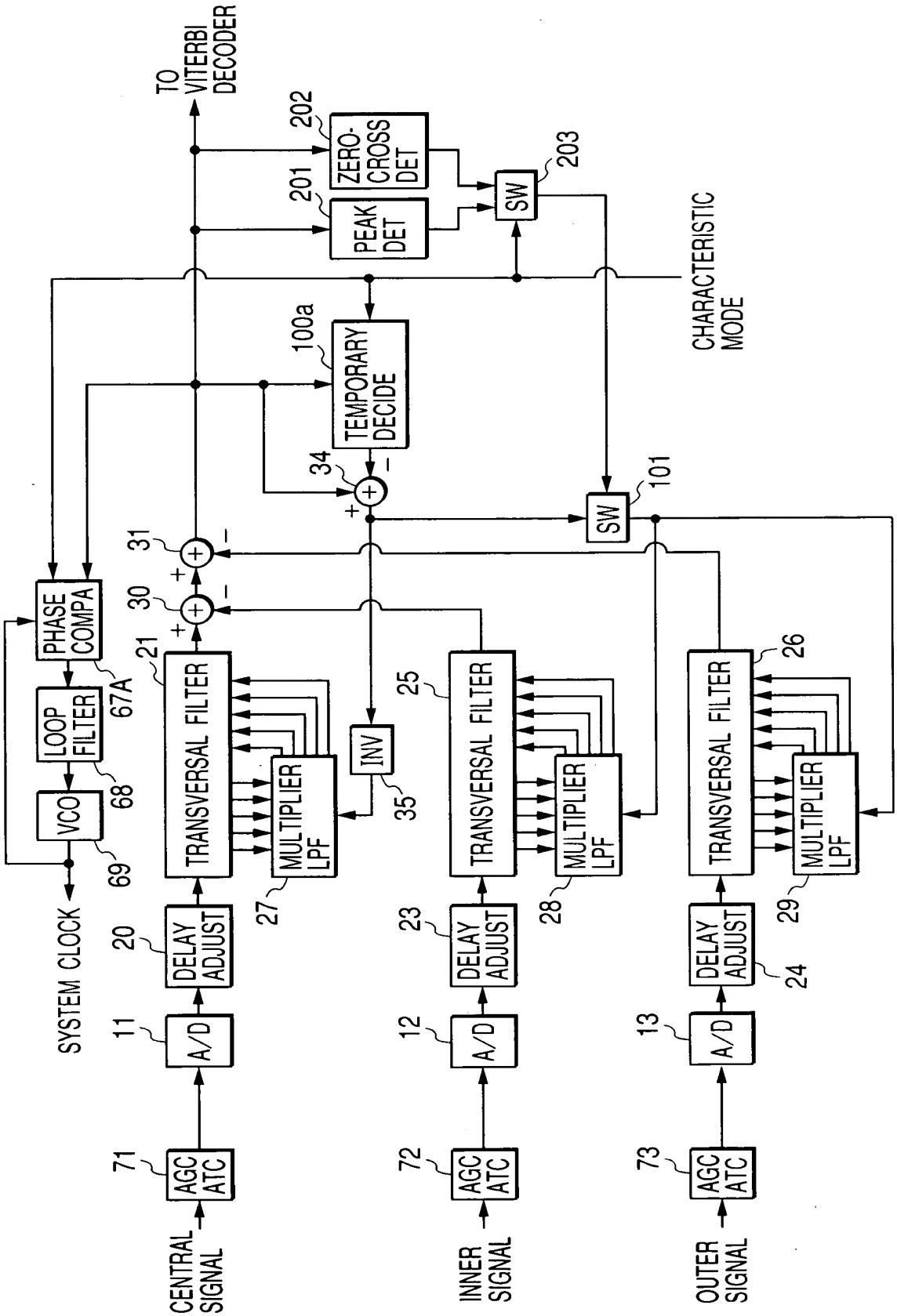

TO VITERBI DECODER
202
ZERO-CROSS DET
201
PEAK DET
203
SW
CHARACTERISTIC MODE
100a
TEMPORARY DECIDE
34
101
SW
31
30
PHASE COMPA
67A
LOOP FILTER
68
VCO
69
SYSTEM CLOCK
21
TRANSVERSAL FILTER
MULTIPLIER LPF
27
INV
35
25
TRANSVERSAL FILTER
MULTIPLIER LPF
28
26
TRANSVERSAL FILTER
MULTIPLIER LPF
29
20
DELAY ADJUST
23
DELAY ADJUST
24
DELAY ADJUST
11
A/D
12
A/D
13
A/D
71
AGC ATC
72
AGC ATC
73
AGC ATC
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL

FIG. 58

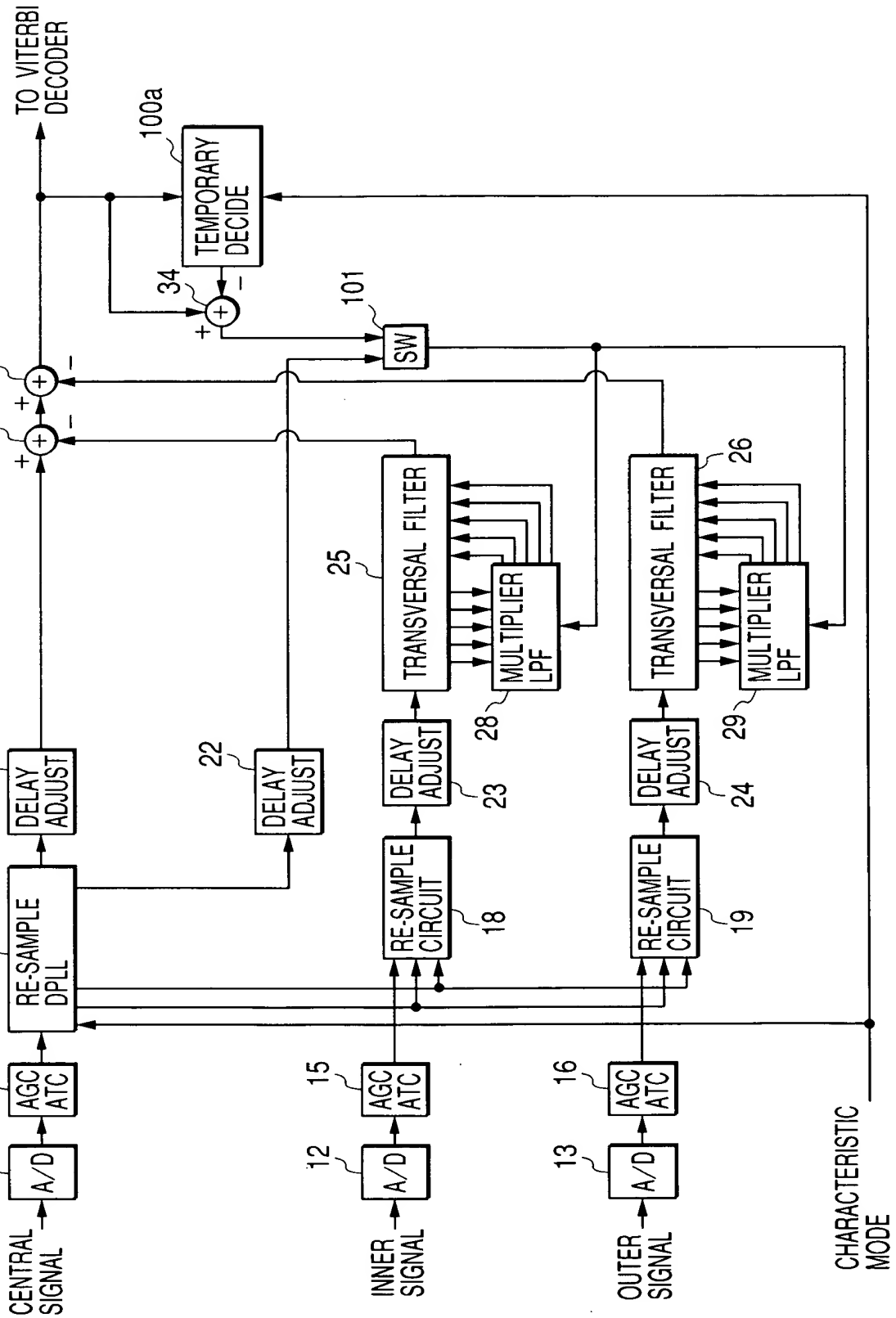

TO VITERBI DECODER
100a
TEMPORARY DECIDE
34
101
SW
31
30
25
TRANSVERSAL FILTER
MULTIPLIER LPF
28
26
TRANSVERSAL FILTER
MULTIPLIER LPF
29
20
DELAY ADJUST
22
DELAY ADJUST
DELAY ADJUST
23
DELAY ADJUST
24
17a
RE-SAMPLE DPLL
RE-SAMPLE CIRCUIT
18
RE-SAMPLE CIRCUIT
19
14
AGC ATC
15
AGC ATC
16
AGC ATC
11
A/D
12
A/D
13
A/D
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL
CHARACTERISTIC MODE

FIG. 59

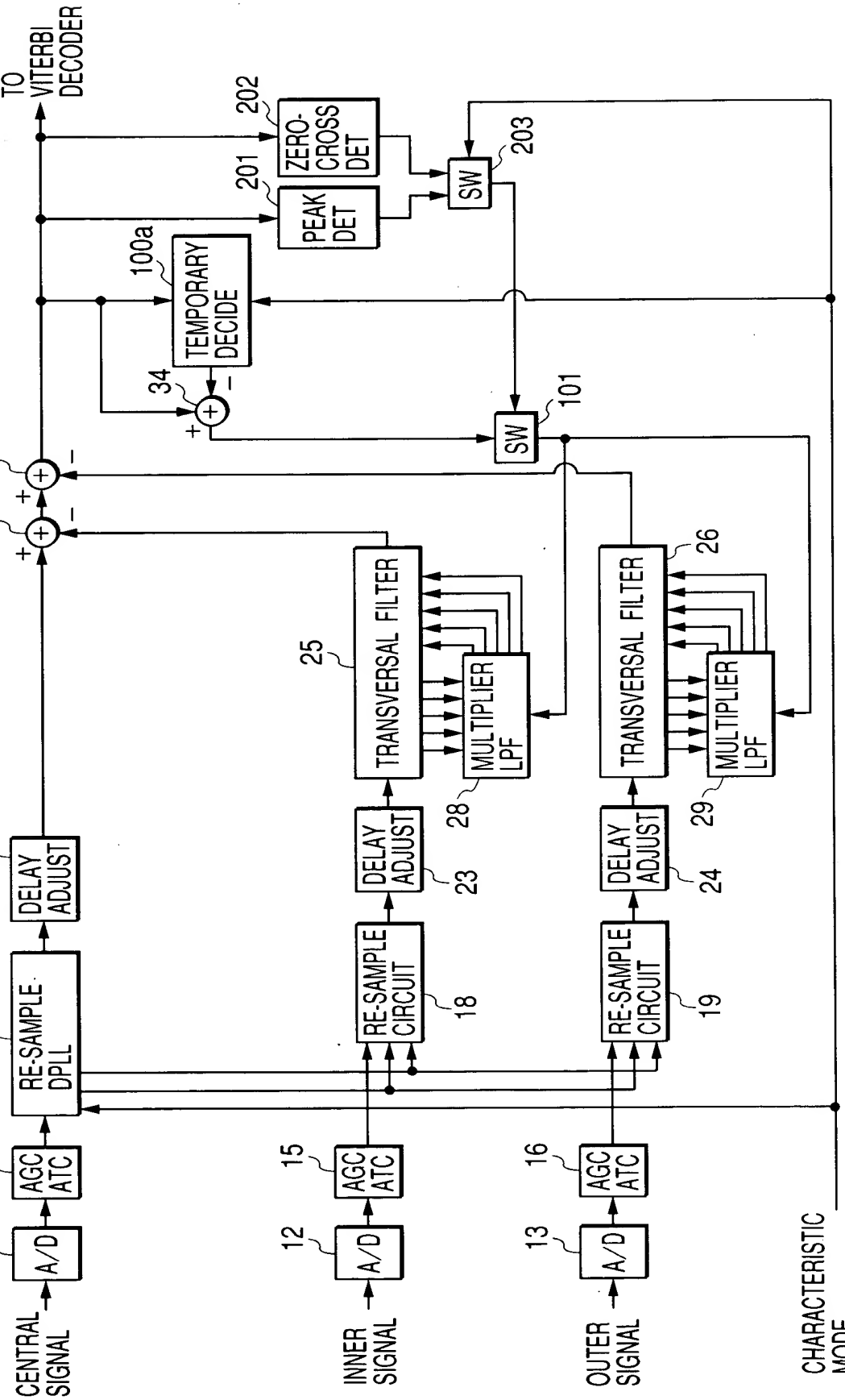

TO VITERBI DECODER
ZERO-CROSS DET
PEAK DET
SW
TEMPORARY DECIDE
SW
TRANSVERSAL FILTER
MULTIPLIER LPF
TRANSVERSAL FILTER
MULTIPLIER LPF
DELAY ADJUST
DELAY ADJUST
DELAY ADJUST
RE-SAMPLE CIRCUIT
RE-SAMPLE CIRCUIT
RE-SAMPLE DPLL
AGC ATC
AGC ATC
AGC ATC
A/D
A/D
A/D
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL
CHARACTERISTIC MODE

FIG. 60

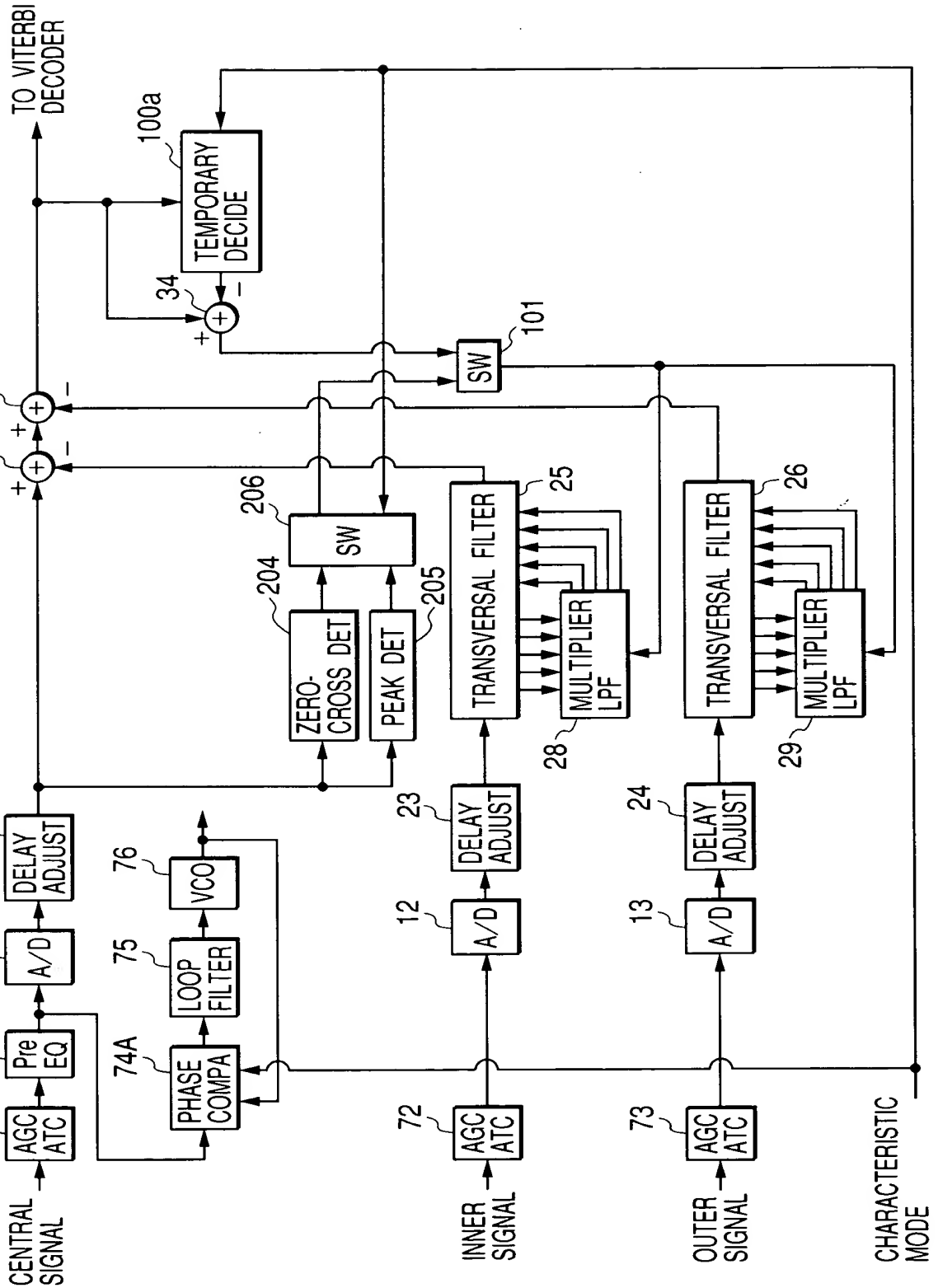

TO VITERBI DECODER
100a
TEMPORARY DECIDE
34
SW
101
31
30
206
SW
204
ZERO-CROSS DET
205
PEAK DET
TRANSVERSAL FILTER
25
MULTIPLIER LPF
28
TRANSVERSAL FILTER
26
MULTIPLIER LPF
29
20
DELAY ADJUST
11
A/D
41
Pre EQ
71
AGC ATC
CENTRAL SIGNAL
74A
PHASE COMPA
75
LOOP FILTER
76
VCO
23
DELAY ADJUST
12
A/D
72
AGC ATC
INNER SIGNAL
24
DELAY ADJUST
13
A/D
73
AGC ATC
OUTER SIGNAL
CHARACTERISTIC MODE

FIG. 61

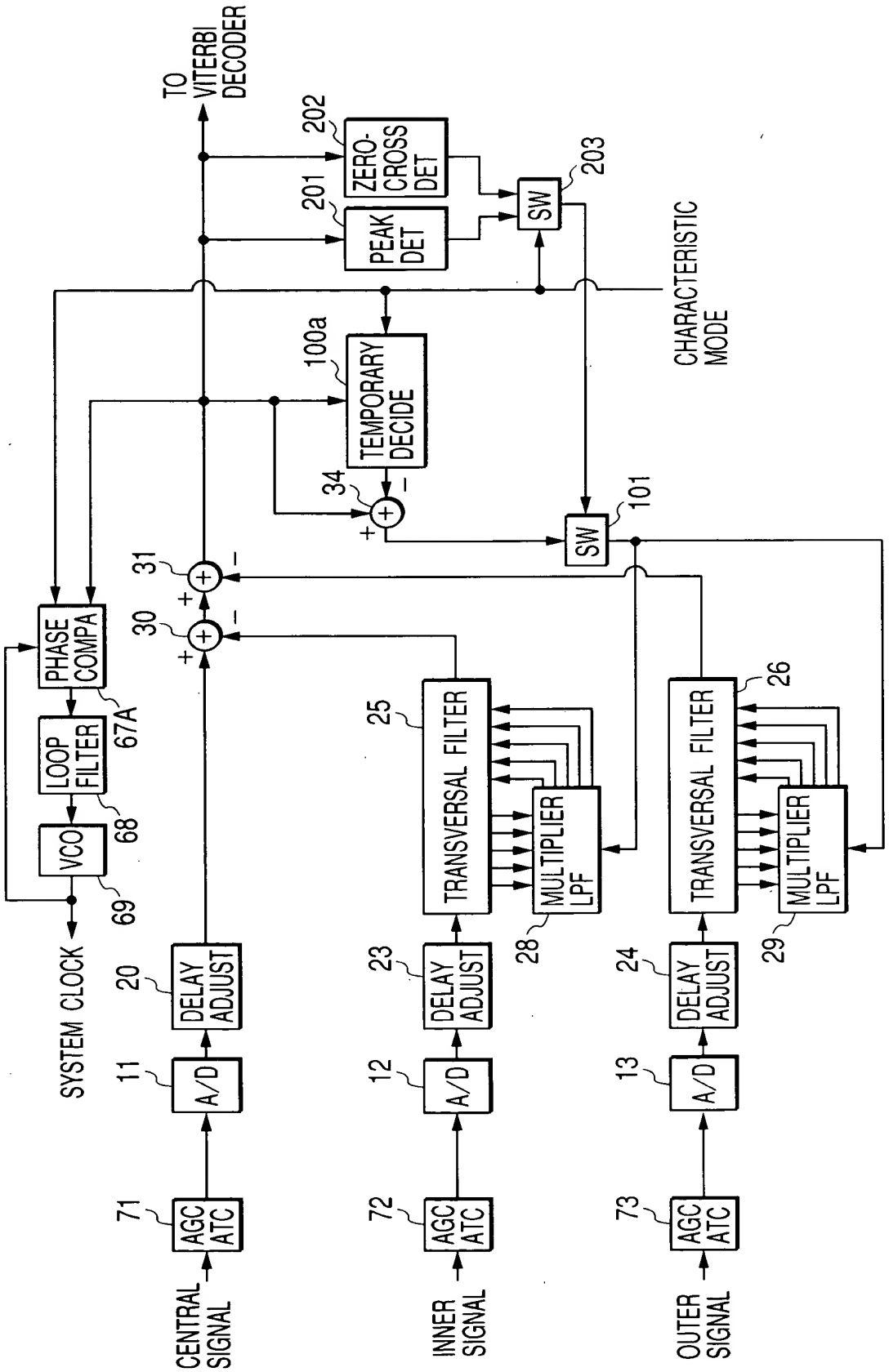

TO VITERBI DECODER
202
ZERO-CROSS DET
201
PEAK DET
SW
203
CHARACTERISTIC MODE
100a
TEMPORARY DECIDE
34
101
31
30
PHASE COMPA
67A
LOOP FILTER
68
VCO
69
SYSTEM CLOCK
25
TRANSVERSAL FILTER
MULTIPLIER LPF
28
26
29
20
23
24
DELAY ADJUST
11
12
13
A/D
71
72
73
AGC ATC
CENTRAL SIGNAL
INNER SIGNAL
OUTER SIGNAL

FIG. 62

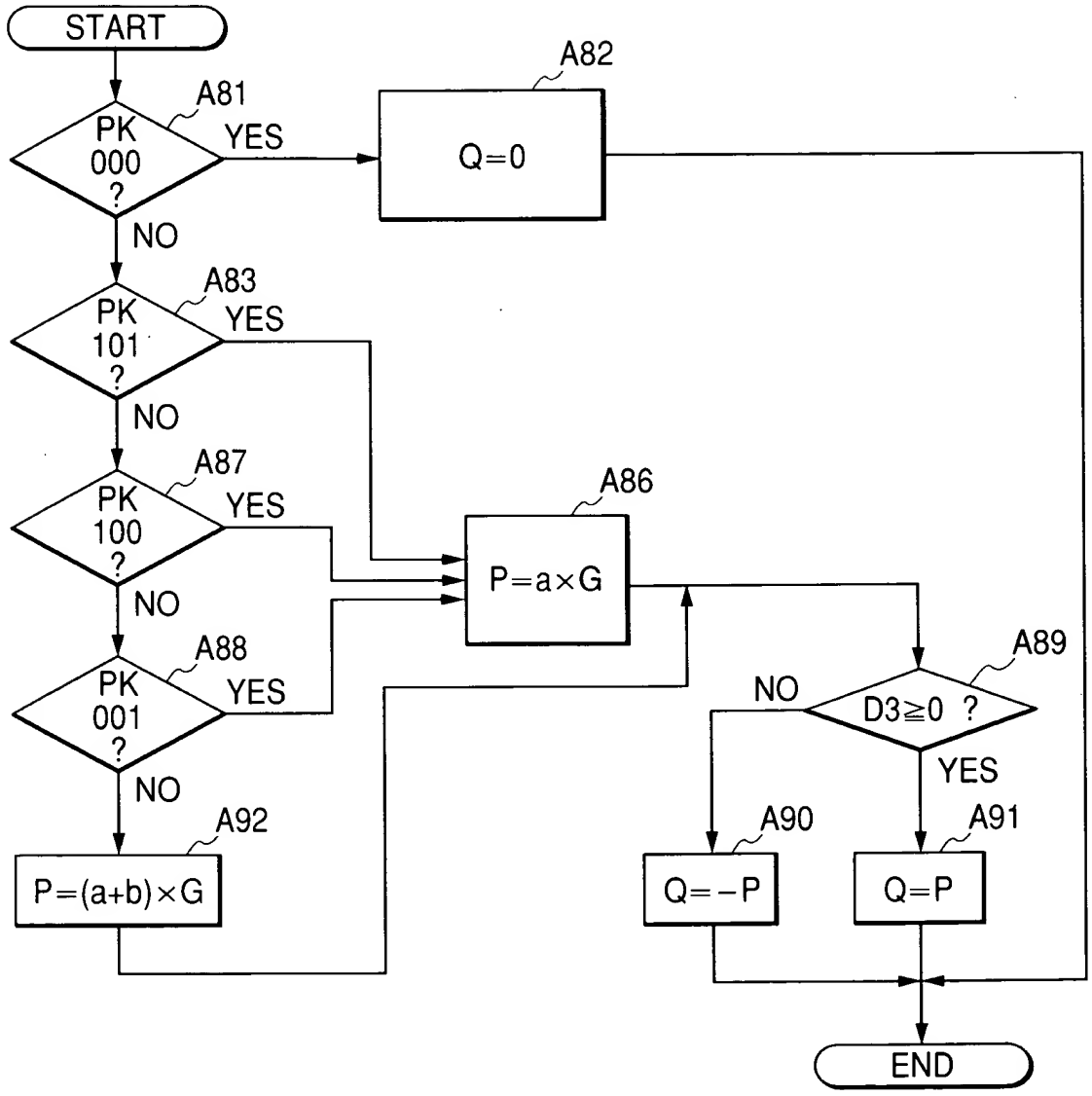
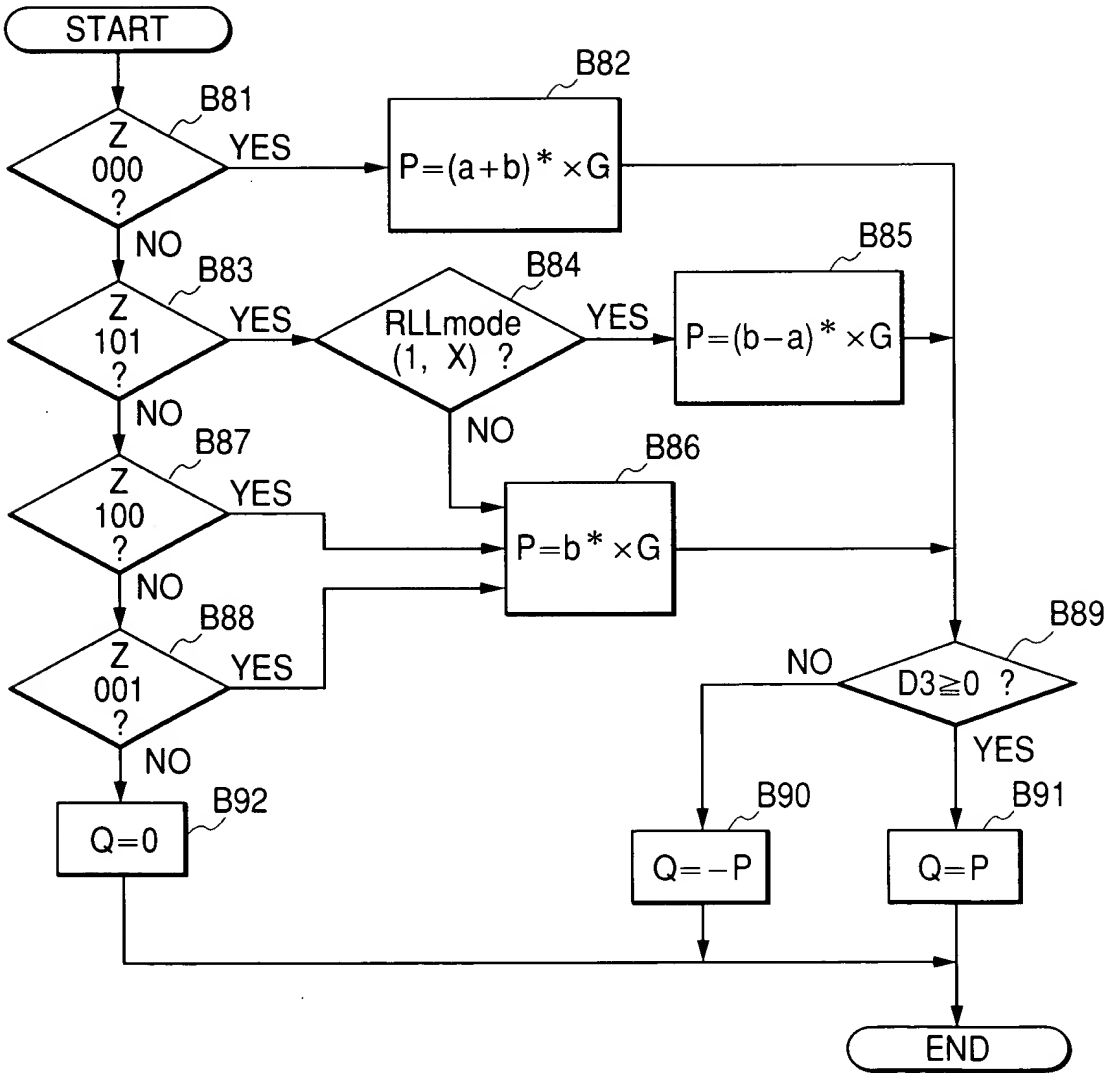

START
A81
PK 000 ?
YES
A82
Q=0
NO
A83
PK 101 ?
YES
NO
A87
PK 100 ?
YES
A86
P=a×G
NO
A88
PK 001 ?
YES
A89
NO
D3≧0 ?
YES
NO
A92
P=(a+b)×G
A90
Q=−P
A91
Q=P
END

FIG. 63


START
B81
Z 000 ?
YES
B82
P=(a+b)*×G
NO
B83
Z 101 ?
YES
B84
RLLmode (1, X) ?
YES
B85
P=(b−a)*×G
NO
B87
Z 100 ?
YES
NO
B86
P=b*×G
B88
Z 001 ?
YES
NO
B89
D3≧0 ?
NO
YES
B92
Q=0
B90
Q=−P
B91
Q=P
END